

Compal Confidential

Broadwell M/B Schematics Document

Intel ULV Processor with DDR3L

Date : 2015/04/14

Version 1.0

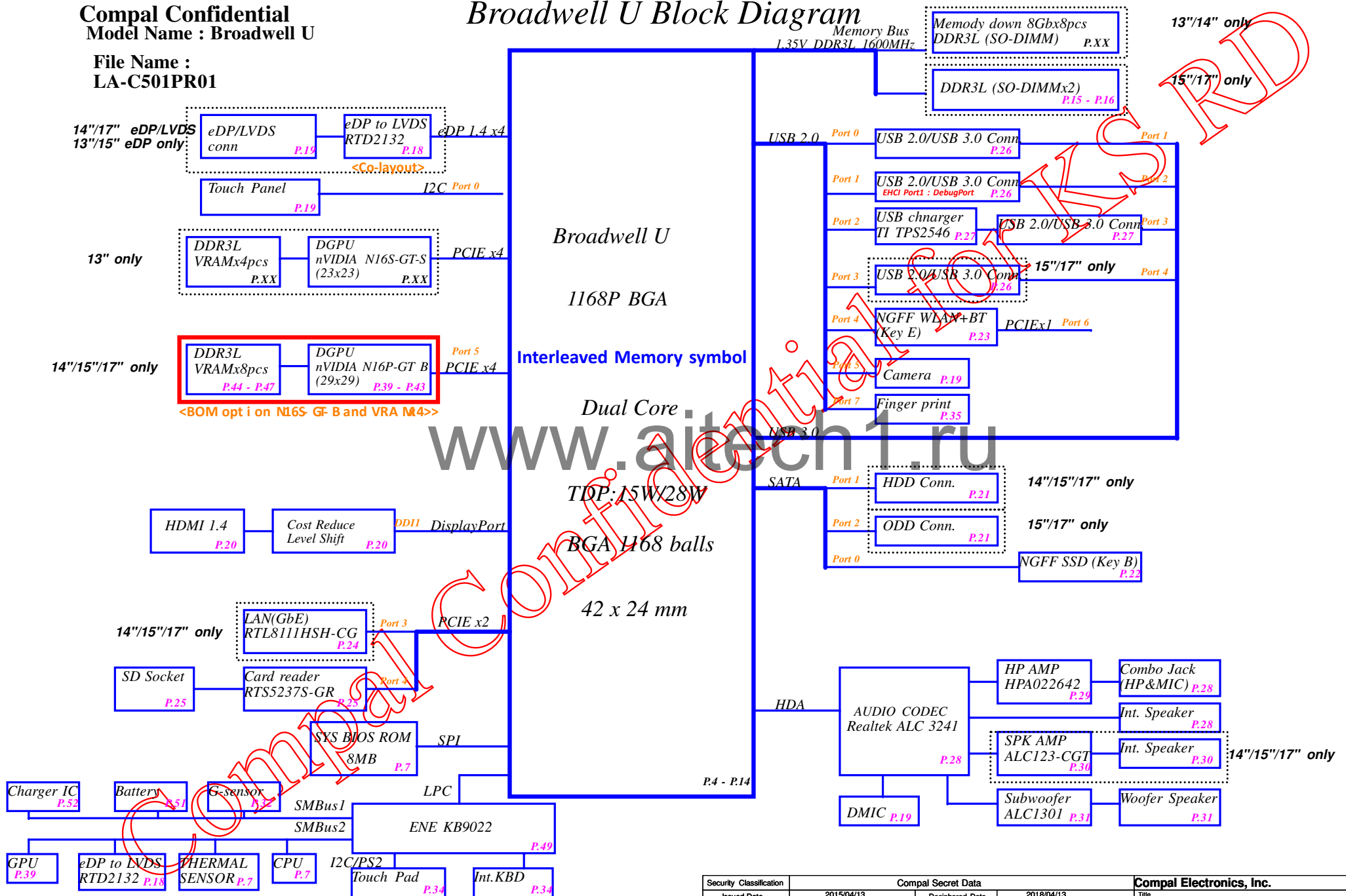
*Project : Puccini (15")
ABW50*

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Model Name : Broadwell U

File Name :
LA-C501PR01

Broadwell U Block Diagram



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Power rail	Control (EC)	Source (CPU)
+RTCVCC	X	X
VIN	X	X
BATT+	X	X
+19VB	X	X
+VL	X	X
+3VL	X	X
+5VALW	EC_ON	X
+3VALW	EC_ON	X
+3VL_EC	EC_ON	X
+3V_PCH	PCH_PWR_EN	X
+1.35V_VDDQ	SYSON	PM_SLP_S5#/PM_SLP_S4#
+SVS	SUSP#	PM_SLP_S3#
+3VS	SUSP#	PM_SLP_S3#
+1.5VS	SUSP#	PM_SLP_S3#
+1.05VS	SUSP#	PM_SLP_S3#
+0.6V_0.675VS	SUSP#	
+VCC_CORE	X	VR12.5_VR_ON

@ is NO SMT part (empty)
short@ : short pad , don't pop.
@EMI@, @ESD@, @RF@ : Reserve , don't pop.
RF@ : RF team request, must add.
EMI@ : EMI team request, must add.
ESD@ : ESD team request, must add.
LVDS@ : Support LVDS panel.
DIS@ : GPU BOM conf i g

ZZZ
PCB
Part Number = DA21D00100
PCB 100 LA-C501P REV0 M8 4

45@	ROYALTY HDMI W/LOGO
Part Number	Description
8000000003HM	8000000003HM
8000000003HM	8000000003HM

SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SOC_SMBCLK SOC_SMBDATA	+3VS	DIMMA	0xA0	TBC	TBC
	+3V_PCH	DIMMB	0xA4	TBC	TBC
SOC_SML0CLK SOC_SML0DATA	+3V_PCH	NA	NA	TBC	TBC
	+3VS	EC	0x1A 0x19	TBC	TBC
SOC_SML1CLK SOC_SML1DATA	+3VS	DGPU	0x96	TBC	TBC
		Thermal Sensor	0x4C	TBC	TBC
		LVDS	0x94~97 0x6A 0x6B	TBC	TBC

<USB2.0 port>

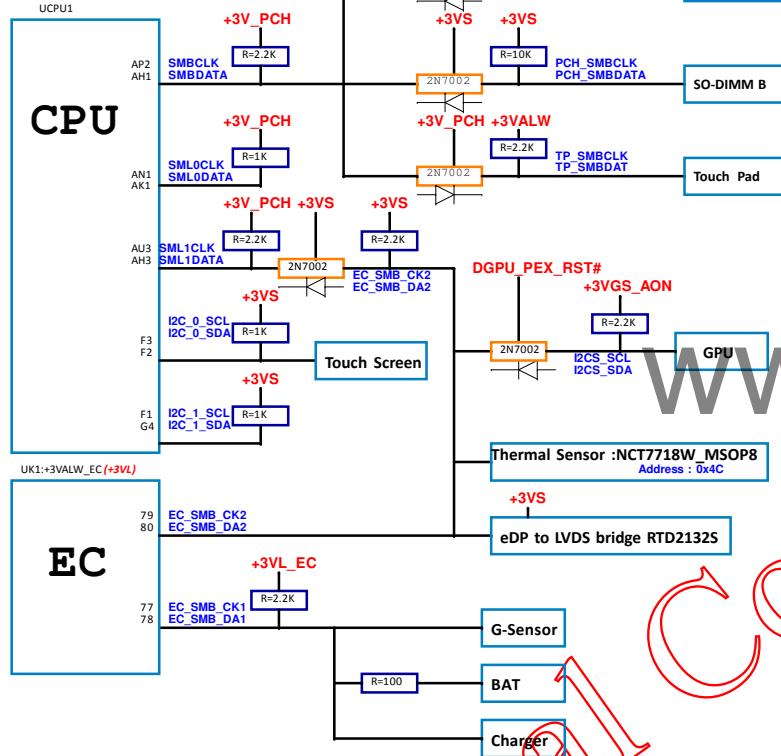
USB2.0 port	DESTINATION	
	UMA	Dis
0	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
1	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
2	USB 2.0/3.0(left side)	USB 2.0/3.0(left side)
3	USB 2.0/3.0(right side)	USB 2.0/3.0(right side)
4	WLAN/BT	WLAN/BT
5	Camera	Camera
6	X	X
7	FingerPrint	FingerPrint

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBUS Port 1	+3VLP_EC	BAT	0x14 0x15	TBC	TBC
		CHGR	0x12	TBC	TBC
		G sensor	0x20	TBC	TBC
SMBUS Port 2					

<PCI-E, SATA, USB3.0>

Lane#	PCI-E	SATA	USB3.0	DESTINATION	
				UMA	Dis
1			1	USB3.0	USB3.0
2			2	USB3.0	USB3.0
3	1		3	USB3.0	USB3.0
4	2		4	USB3.0	USB3.0
5	3			10/100/1000 LAN	10/100/1000 LAN
6	4			Card reader(PCI-E)	Card reader(PCI-E)
7				GPU(DIS only)	GPU(DIS only)
8				GPU(DIS only)	GPU(DIS only)
9				GPU(DIS only)	GPU(DIS only)
10				GPU(DIS only)	GPU(DIS only)
11	L0	3		WLAN	WLAN
12	L1	2		ODD	ODD
13	L2	1		HDD	HDD
14	L3	0		SSD	SSD



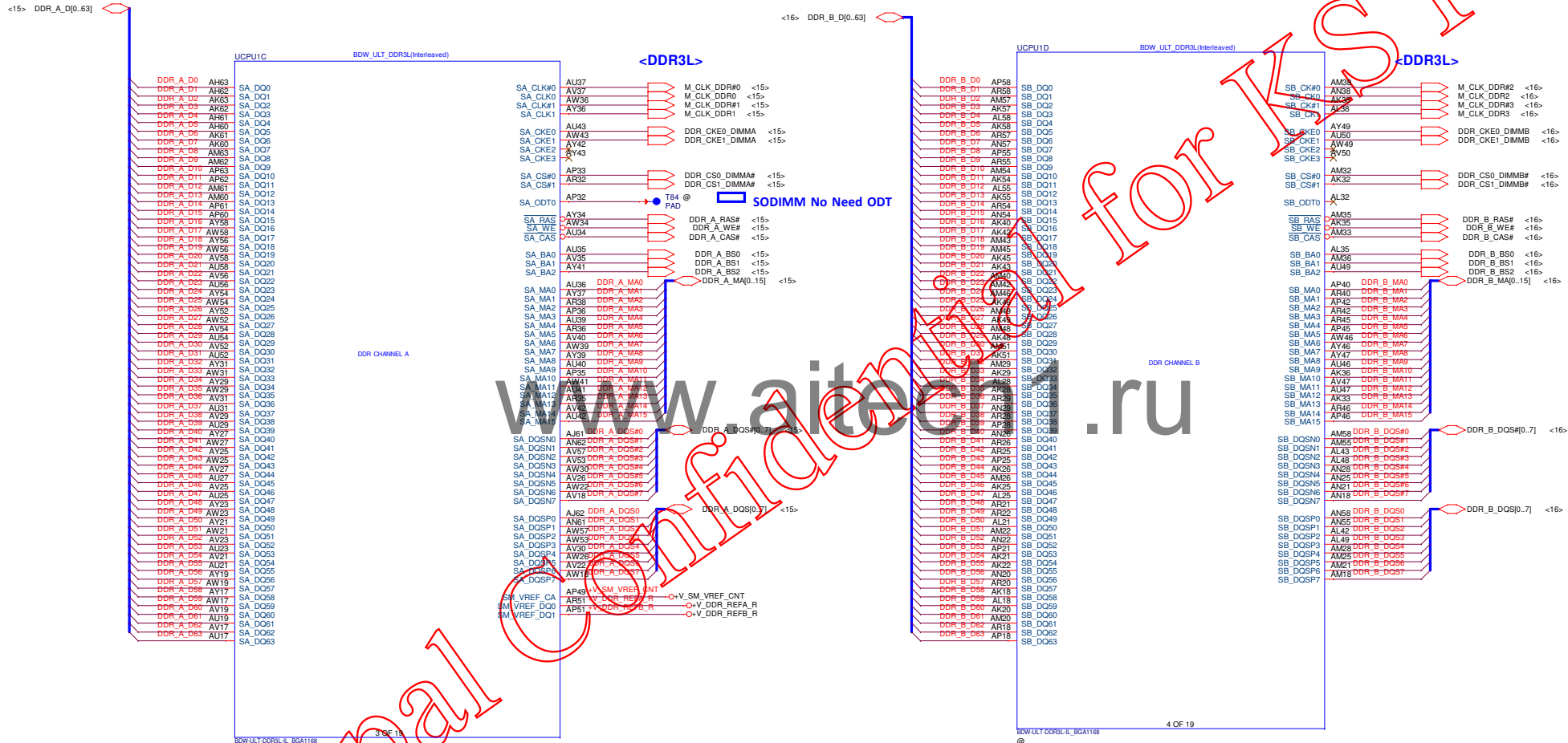
I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C 0	+3VS	Touch Panel	0x20	TBC	TBC
I2C 1	+3VS	NA	TBC	TBC	TBC

CPU Memory down vender control table

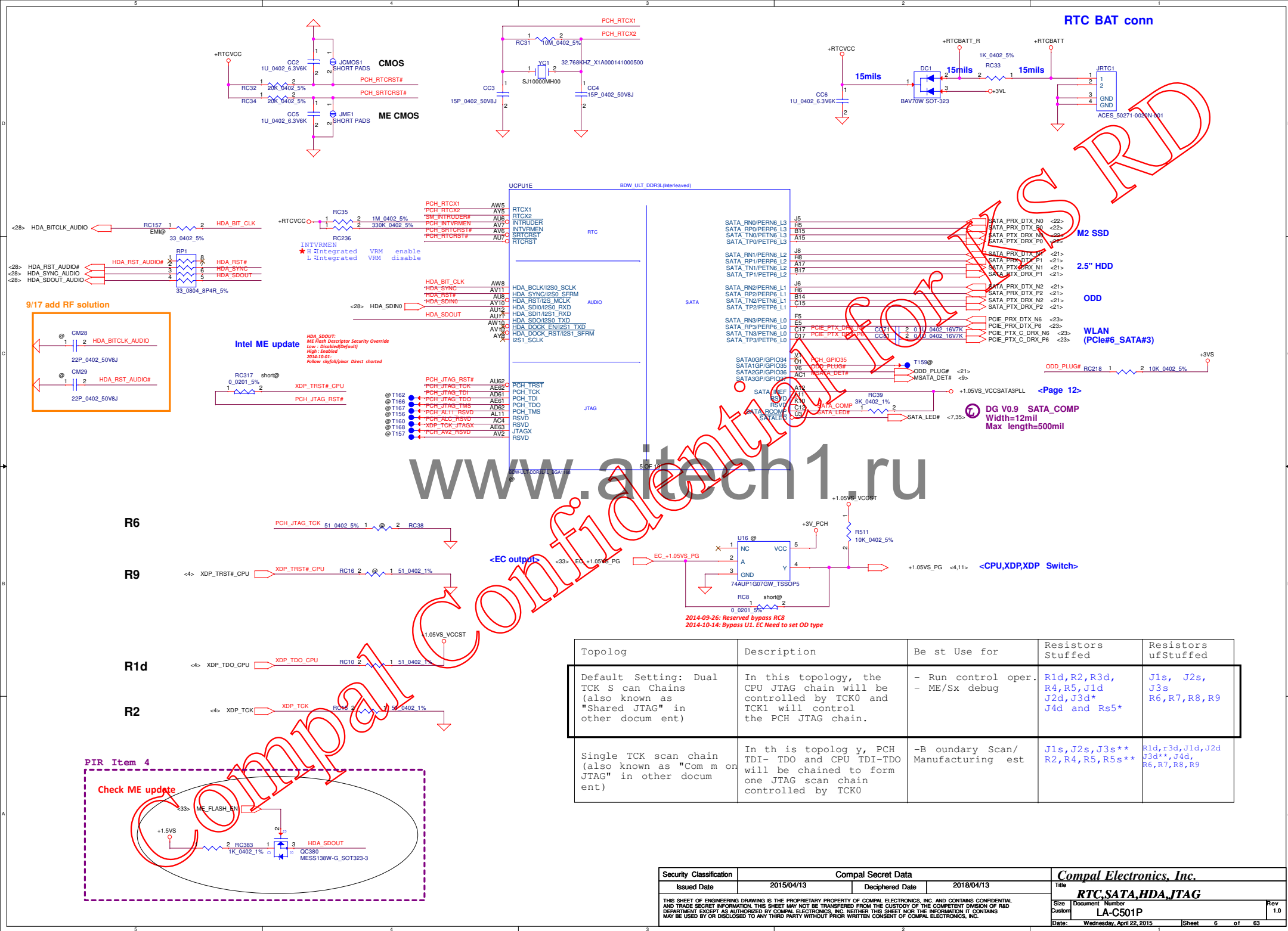
CPU_GPIO50 SDRAM_ID4	CPU_GPIO49 SDRAM_ID3	CPU_GPIO48 SDRAM_ID2	CPU_GPIO47 SDRAM_ID1	Vender	MD size	Vender descpt i on Note	Project
0	0	0	0	X	X	X	SODIMMx2 (A,B) 15"/17"
0	0	0	1	X	X	X	SODIMMx1(A) No MDx16bitx4pcs (B) 13"
0	0	1	0	Micron	256x16	MT41K512M16TNA-125:E	SODIMMx1(A) MDx16bitx4pcs (B) 13"
0	0	1	1	Samsung	256x16	4B8G1646Q-MYK0	SODIMMx1(A) MDx16bitx4pcs (B) 13"
0	1	0	0	Hynix	256x16	HSTC8G63AMR-PBA	SODIMMx1(A) MDx16bitx4pcs (B) 13"
0	1	0	1	Micron	512x8	MT41K512M8RG-107:N	MDx8bitx8pcs (A) SODIMMx1(B) 14"
0	1	1	0	Samsung	512x8	K4B4G0846Q-HYK0	MDx8bitx8pcs (A) SODIMMx1(B) 14"
0	1	1	1	Hynix	512x8	HSTC4G83BFR-PBA	MDx8bitx8pcs (A) SODIMMx1(B) 14"

Interleaved Memory

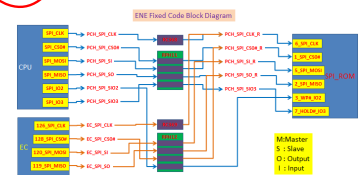
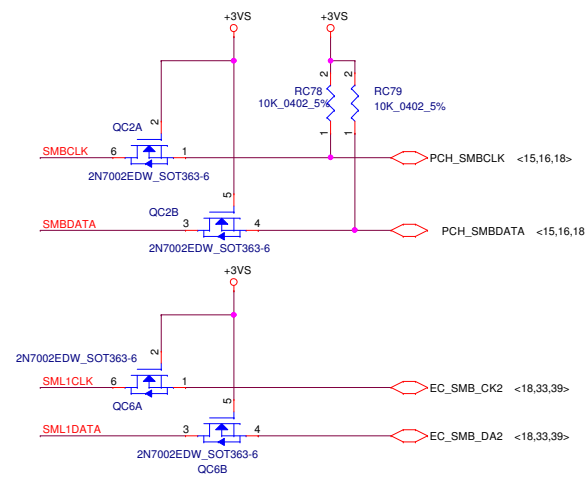
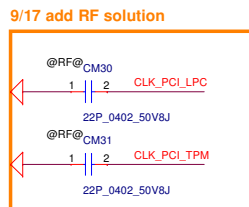
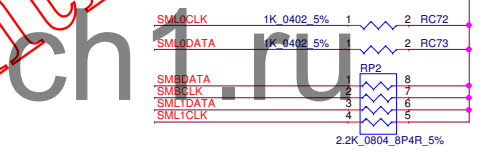
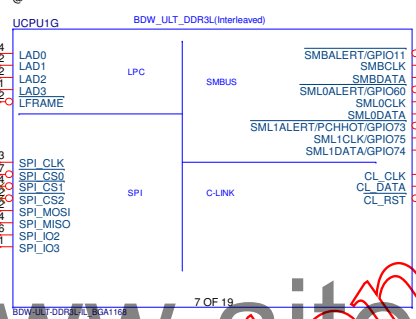
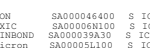
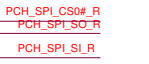
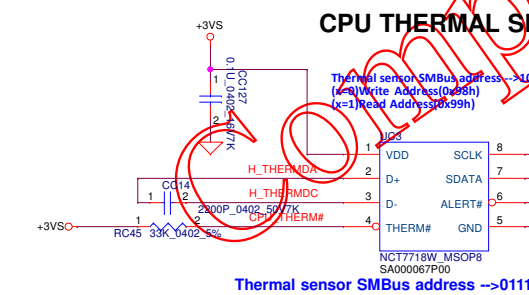


Interleaved Memory

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- Each PQECLKRQ# needs to be routed to PQE Part (n+1) - New to LPT-IP and what is not clear in EDS. Updated in LPT-LP EDS SU Rev1.5.1 (#508767).
- Each CLKOUT PQE5Q can be assigned to any PQECLKRQ#.

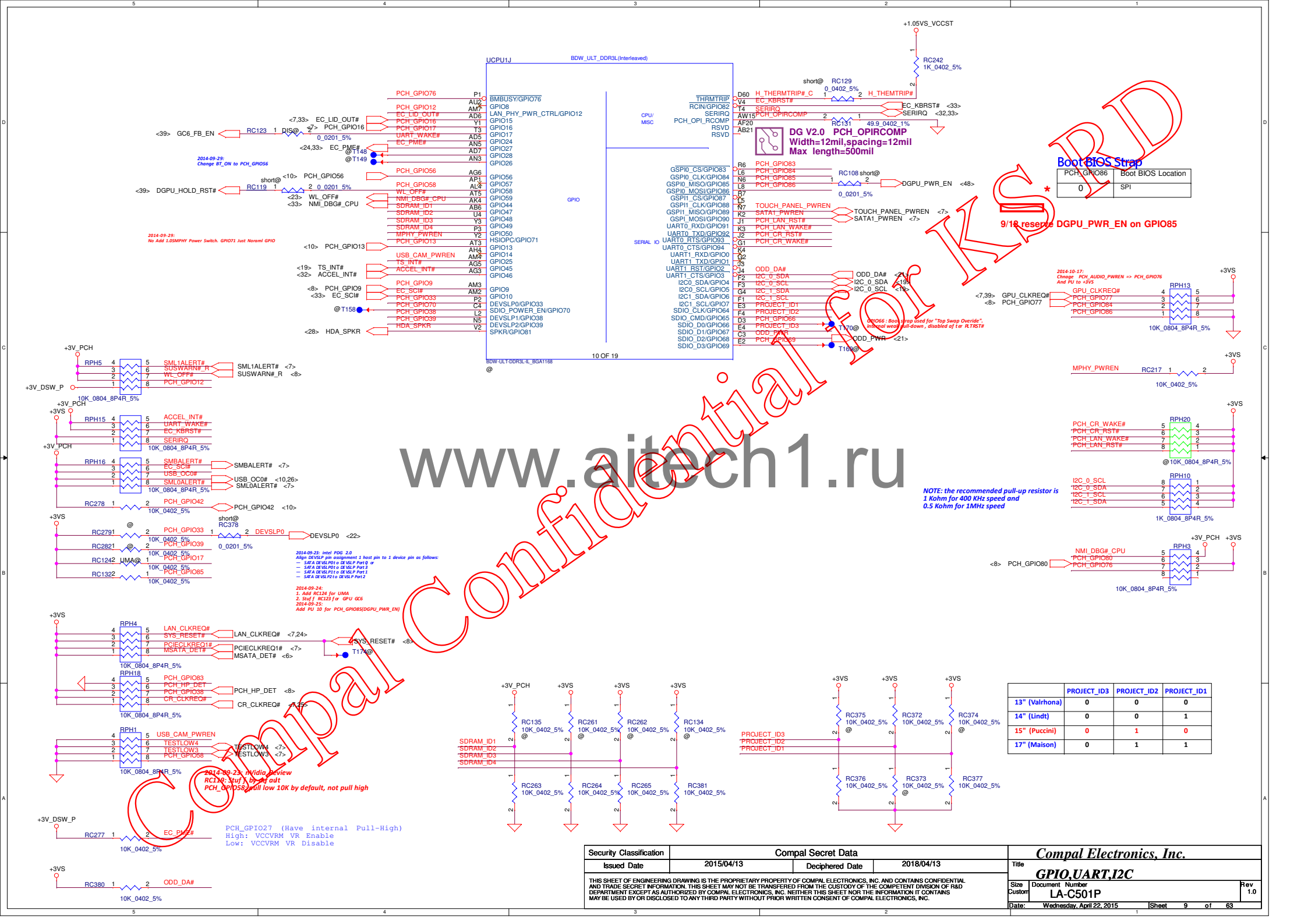


Thermal sensor SMBus address --> 100-1_100xb : 0x4C
(x=0)Write Address(0x98h)
(x=1)Read Address(0x99h)

Thermal sensor SMBus address --> 100-1_100xb : 0x4C
(x=0)Write Address(0x98h)
(x=1)Read Address(0x99h)

Thermal sensor SMBus address -->0111_100xb (0x78h)

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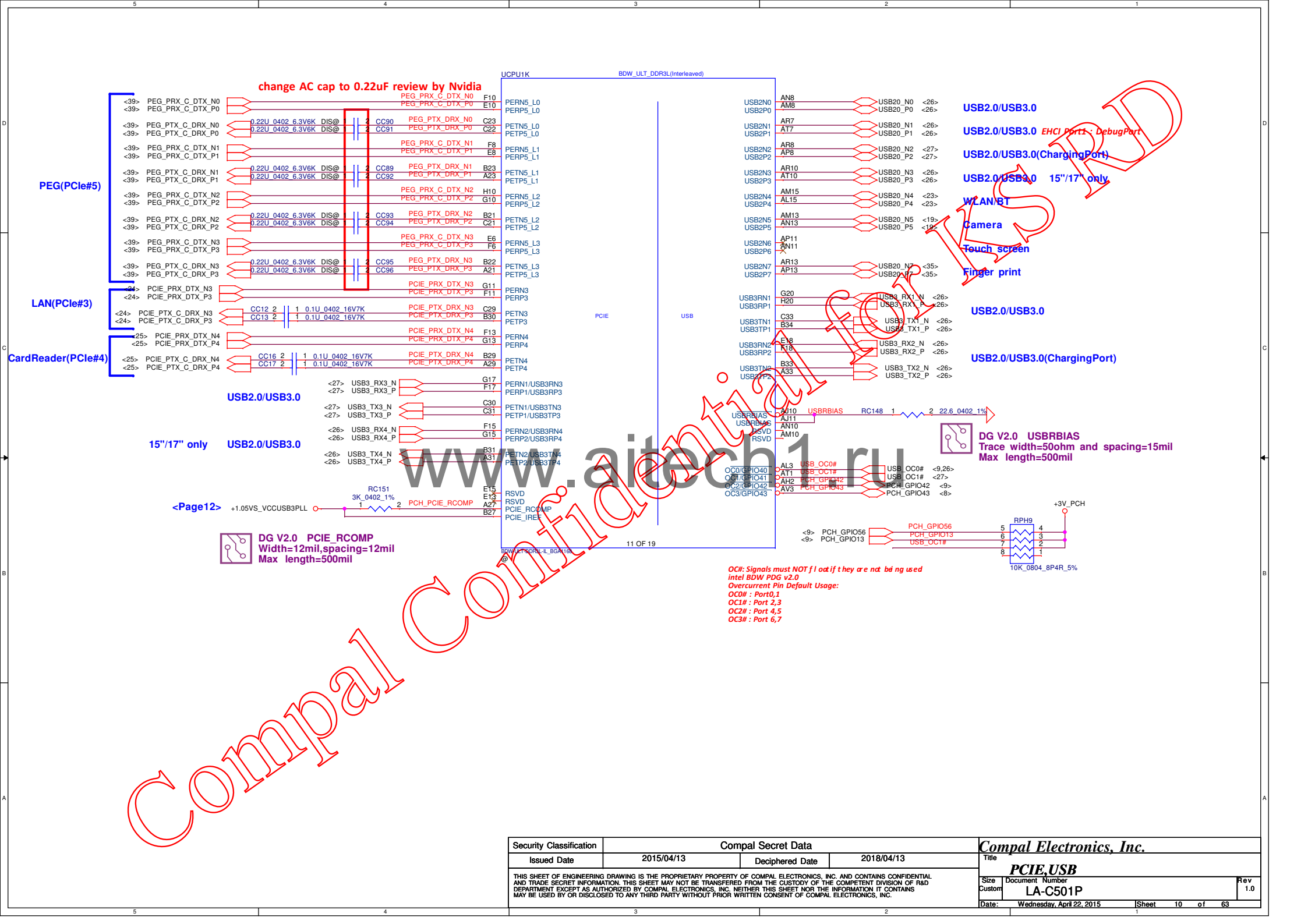
Boot BIOS Strap

PCH_GPIO86	Boot BIOS Location
0	SPI

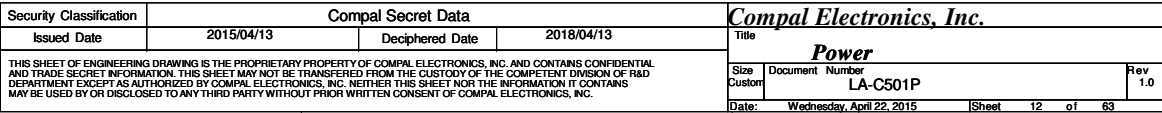
9/18 reserve DGPU_PWR_EN on GPIO85

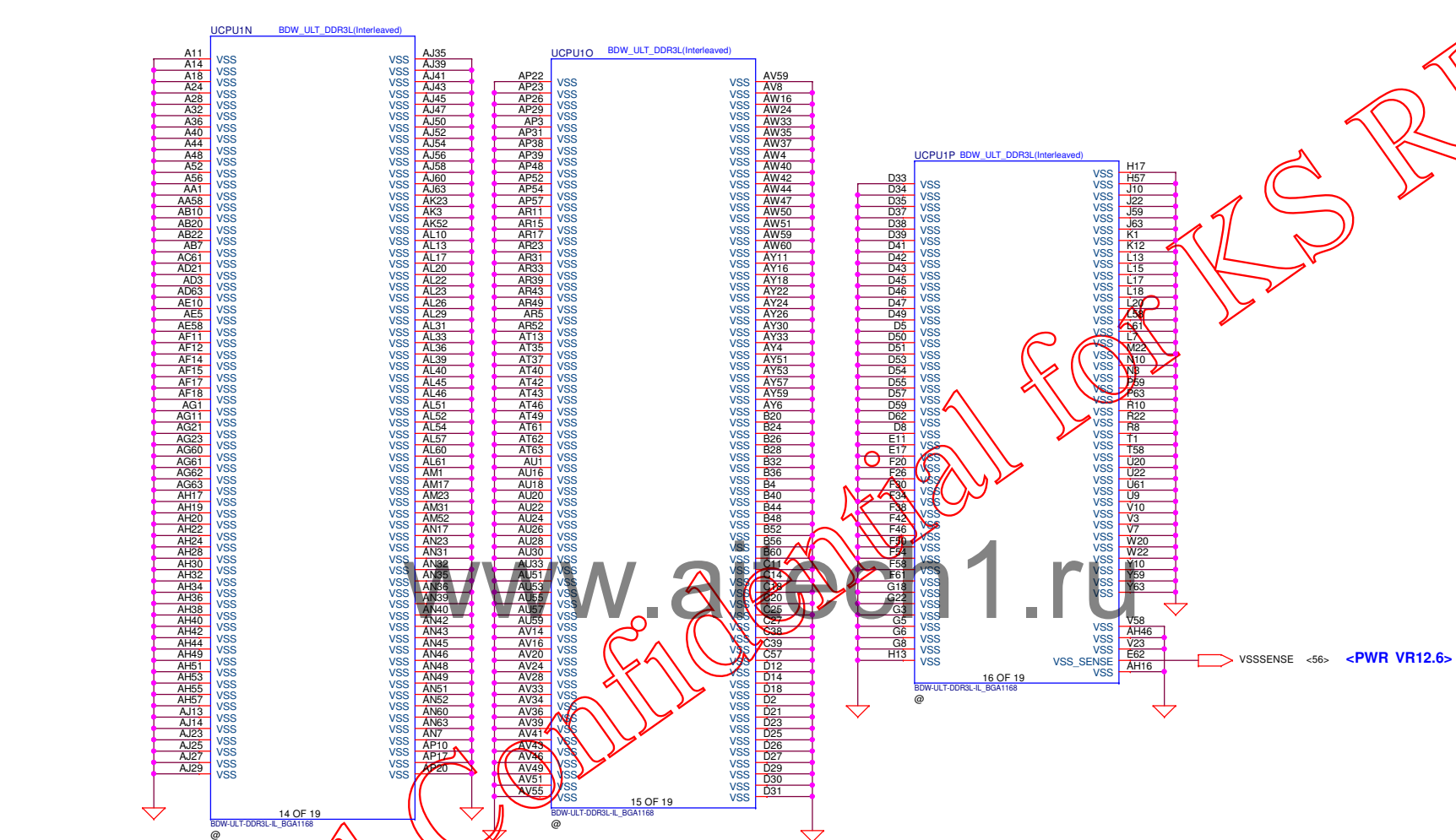
NOTE: the recommended pull-up resistor is 1 Kohm for 400 KHz speed and 0.5 Kohm for 1MHz speed

	PROJECT_ID3	PROJECT_ID2	PROJECT_ID1
13" (Valrhona)	0	0	0
14" (Lindt)	0	0	1
15" (Puccini)	0	1	0
17" (Maison)	0	1	1

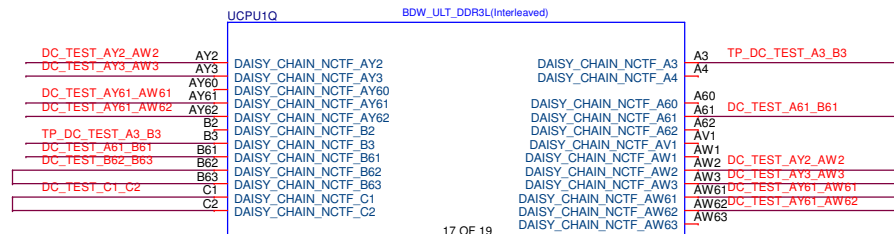


The diagram illustrates the SVID (Serial Voltage Identification) circuit. A voltage divider is connected to the +1.05V_{S_VCCST} supply. The divider consists of a 75.0402_5% resistor (RC154) in series with a 43.0402_1% resistor (RC155). The output of the divider is connected to the H_CPU_SVIDALRT# pin. The input signal is labeled <PWR VR12.6> and the output is labeled <56> VR_SVID_ALRT#.



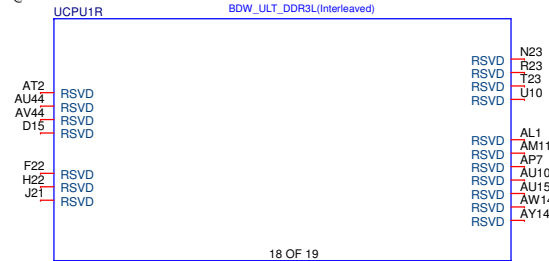


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BDW-ULT-DDR3L-IL_BGA1168

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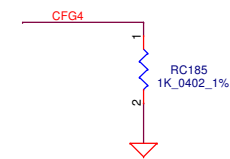


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BDW-ULT-DDR3L-IL_BGA1168

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Display Port Presence Strap

CFG4

- 1 : Disabled; No Physical Display Port attached to Embedded Display Port
- * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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2018/04/13

Title

RSVD/CFG

Size

Document Number

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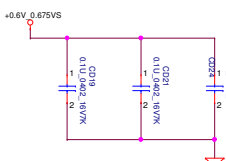
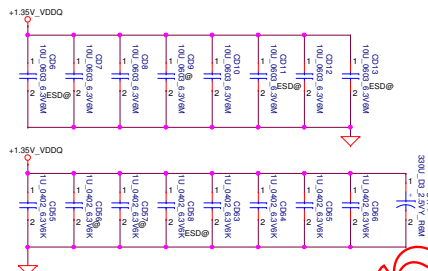
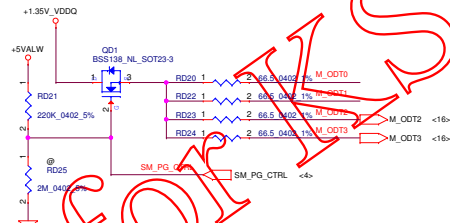
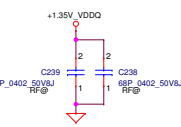
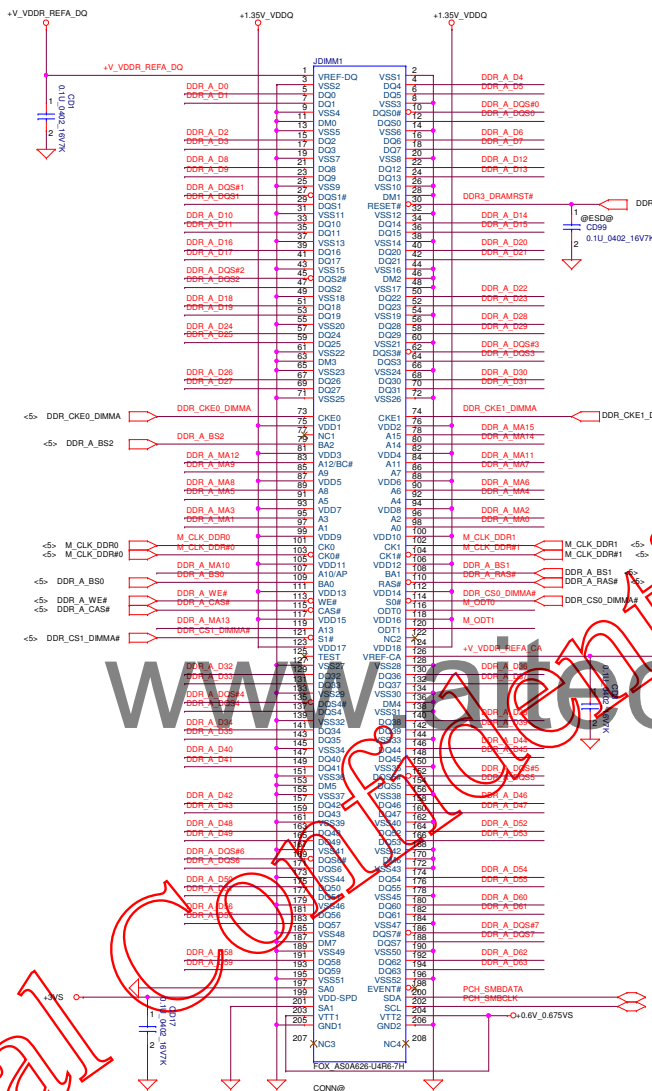
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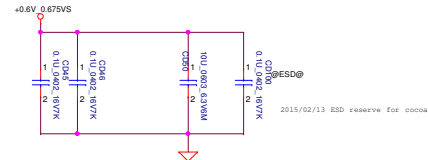
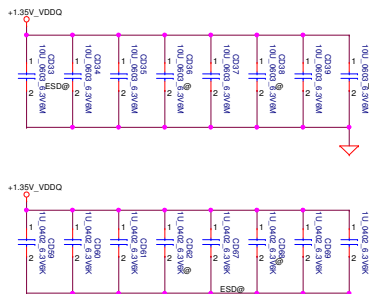
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 <S> DDR_A_DQS[0..7]
 <S> DDR_A_DQS#0..7
 <S> DDR_A_MA[0..15]



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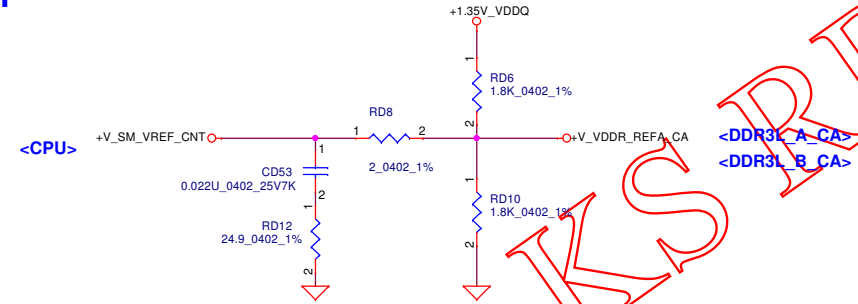
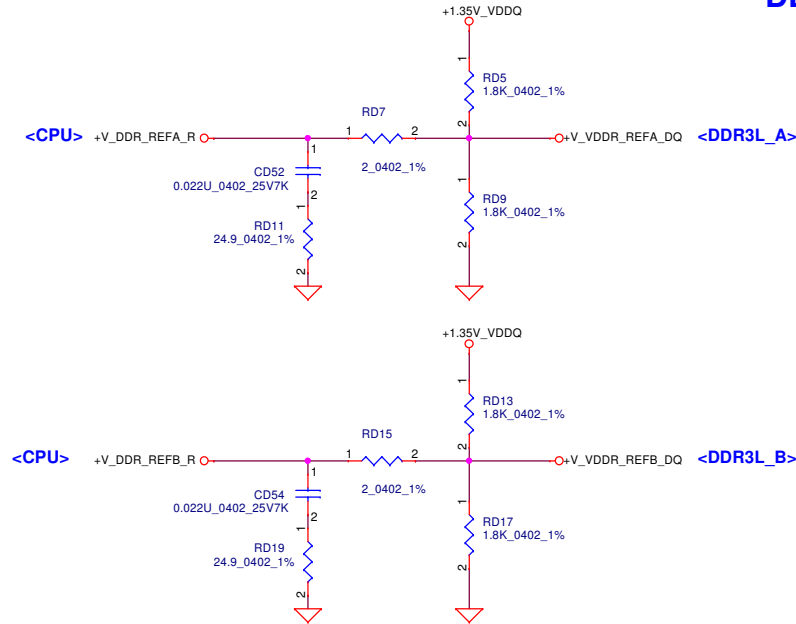
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 <5> DDR_B_DQS[0..7]
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 <5> DDR_B_MA[0..15]



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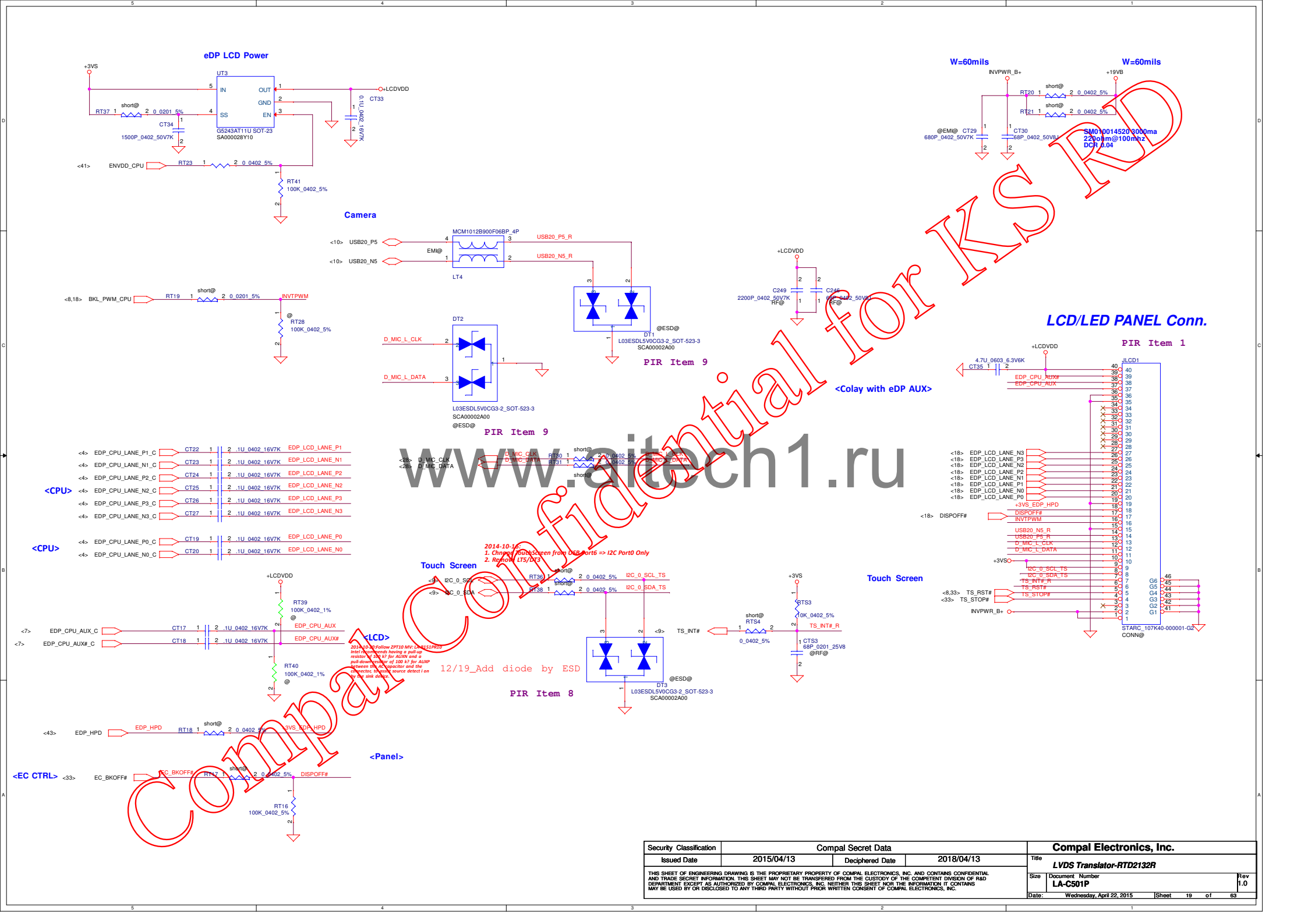
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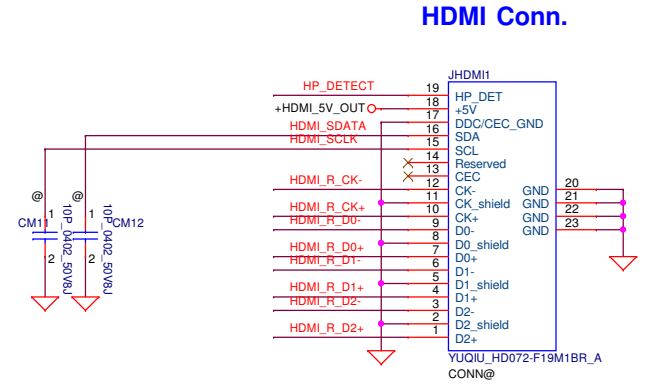
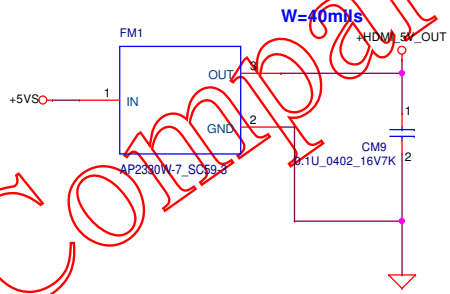
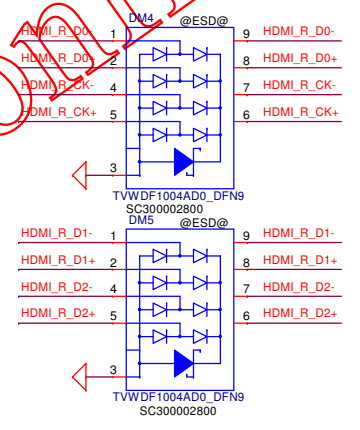
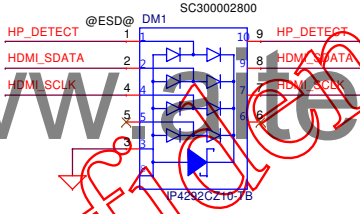
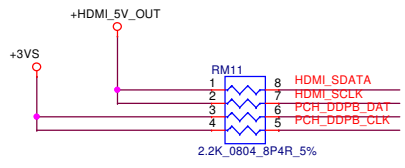
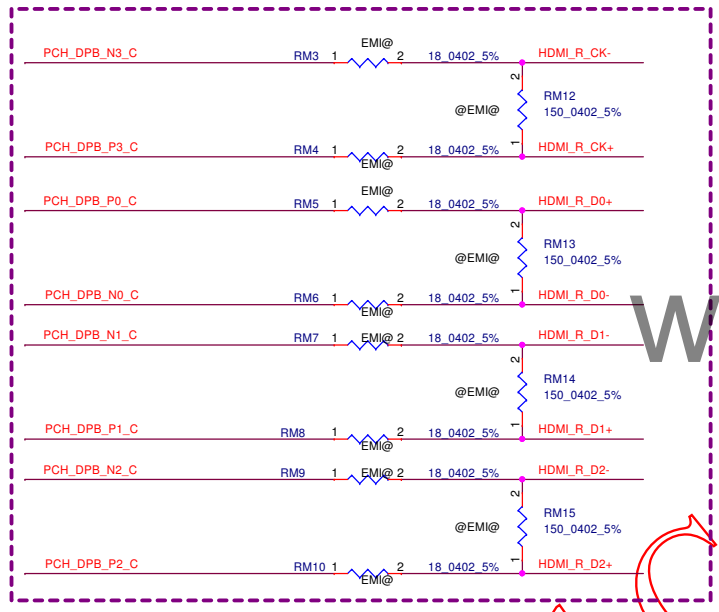
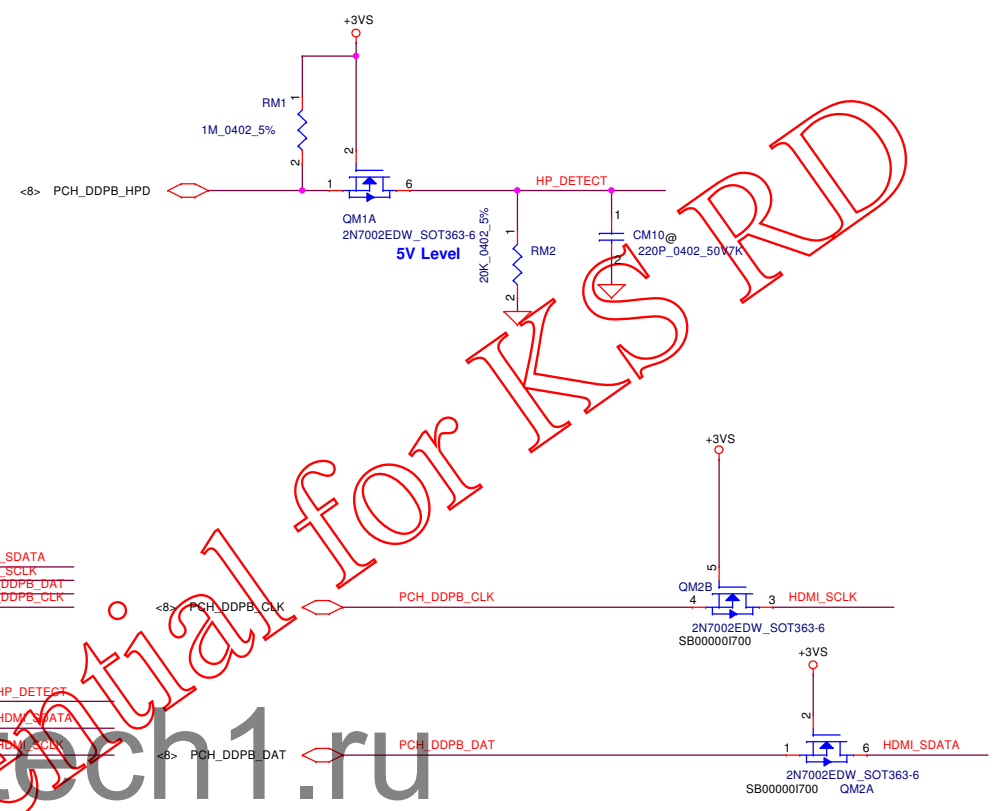
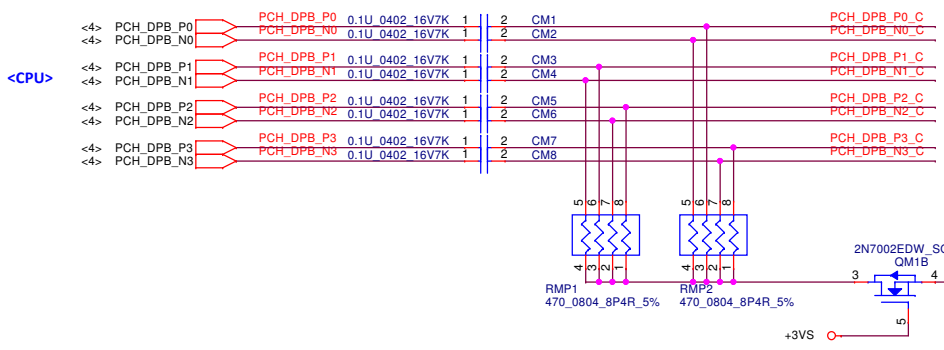
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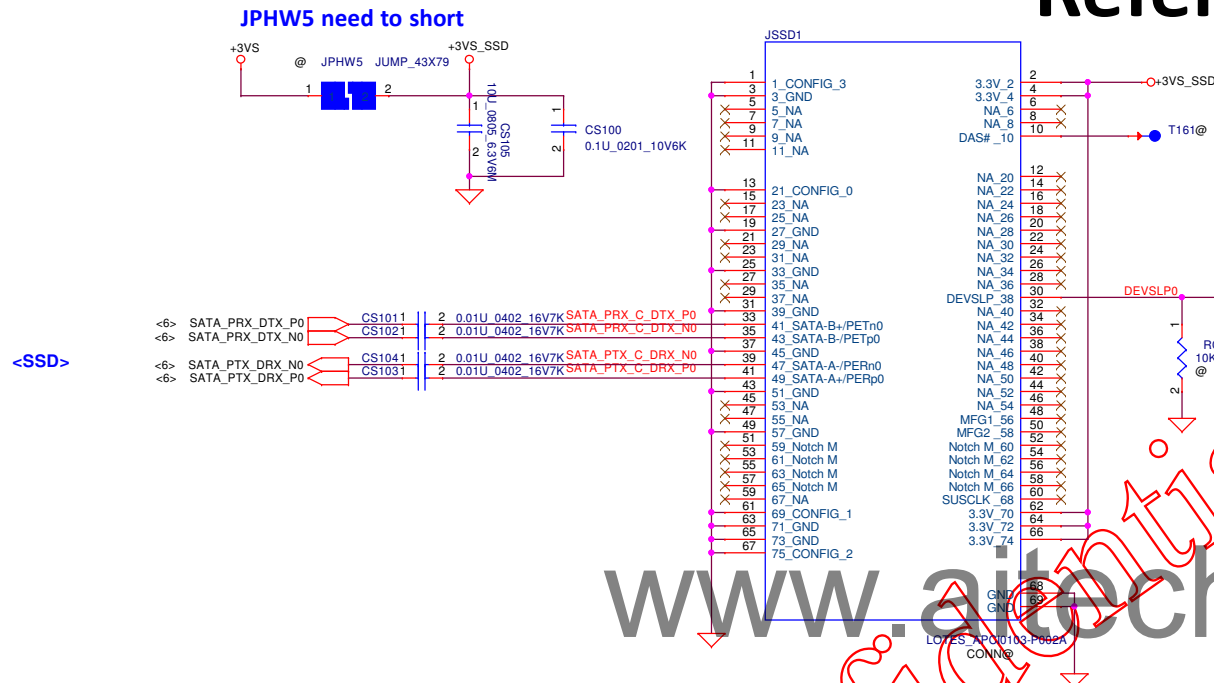


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					of
					63



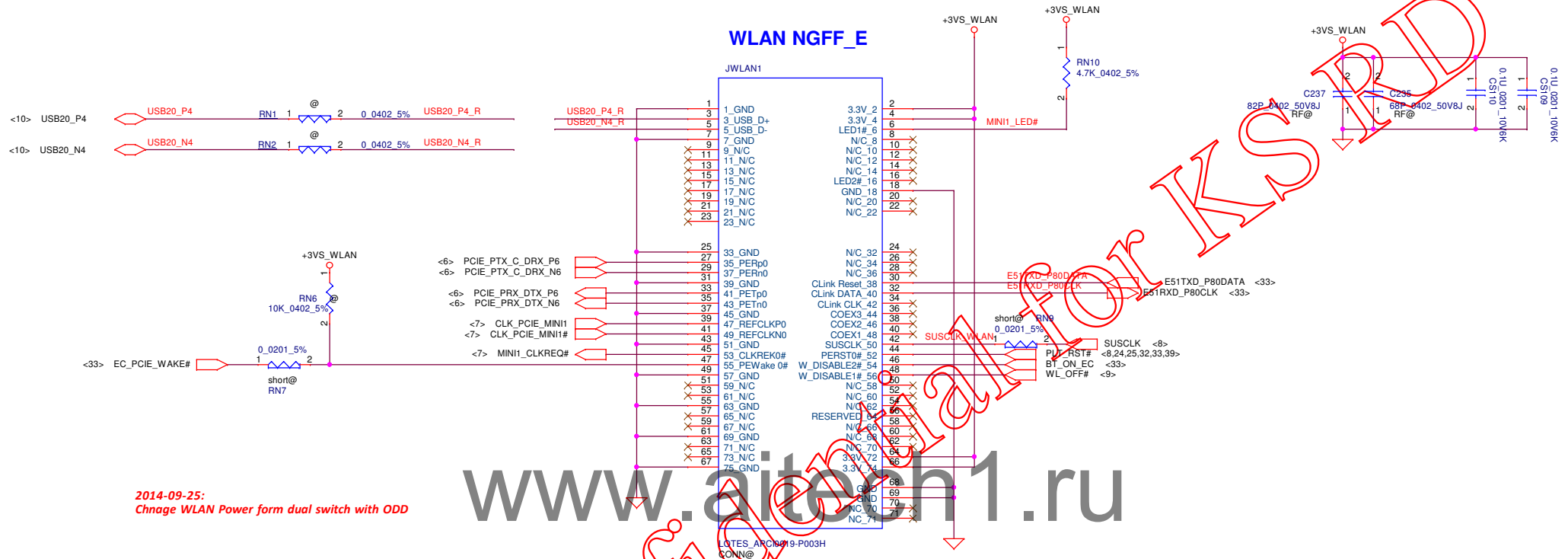
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/04/13	Deciphered Date	2018/04/13	Title	
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Size	Document Number	LA-C501P		Rev	1.0
Date:	Wednesday, April 22, 2015	Sheet	20	of	63

Refer Skyfall test board



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				eDP to CRT	
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				Document Number	1.0
				LA-C501P	
				Date: Wednesday, April 22, 2015	Sheet 22 of 63

Refer Skyfall NGFF



2014-09-25:
Chnage WLAN Power form dual switch with ODD

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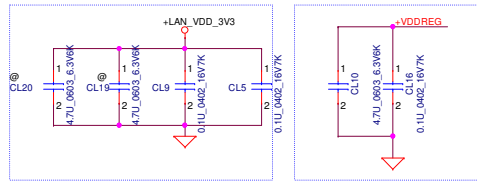
WLAN

NGFF Key_E 67P P0.5 CH 0.32 H2.2 STD

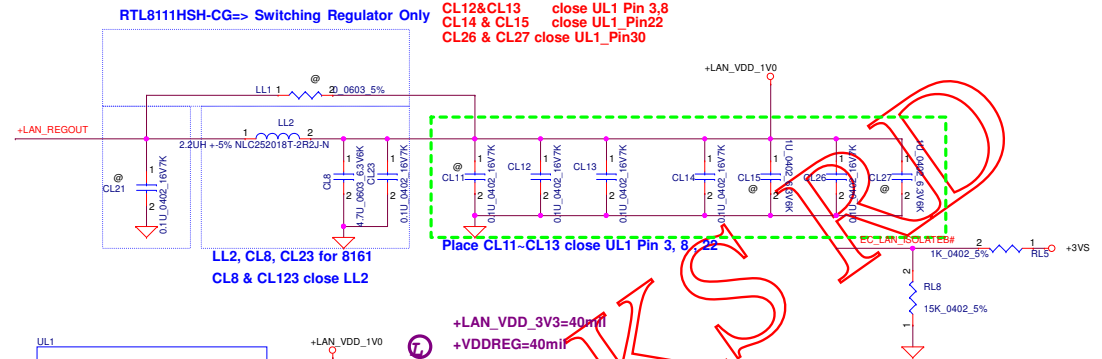
Del +1.5VS_WLAN

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/04/13	Deciphered Date	2018/04/13	Title	WLAN
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					LA-C501P
				Date	Wednesday, April 22, 2015
				Sheet	23 of 63
				Rev	1.0

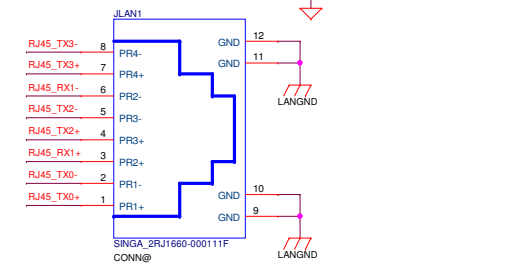
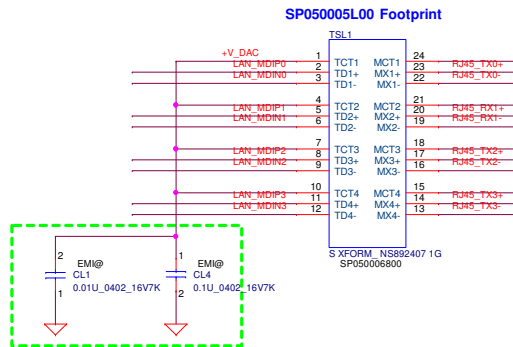
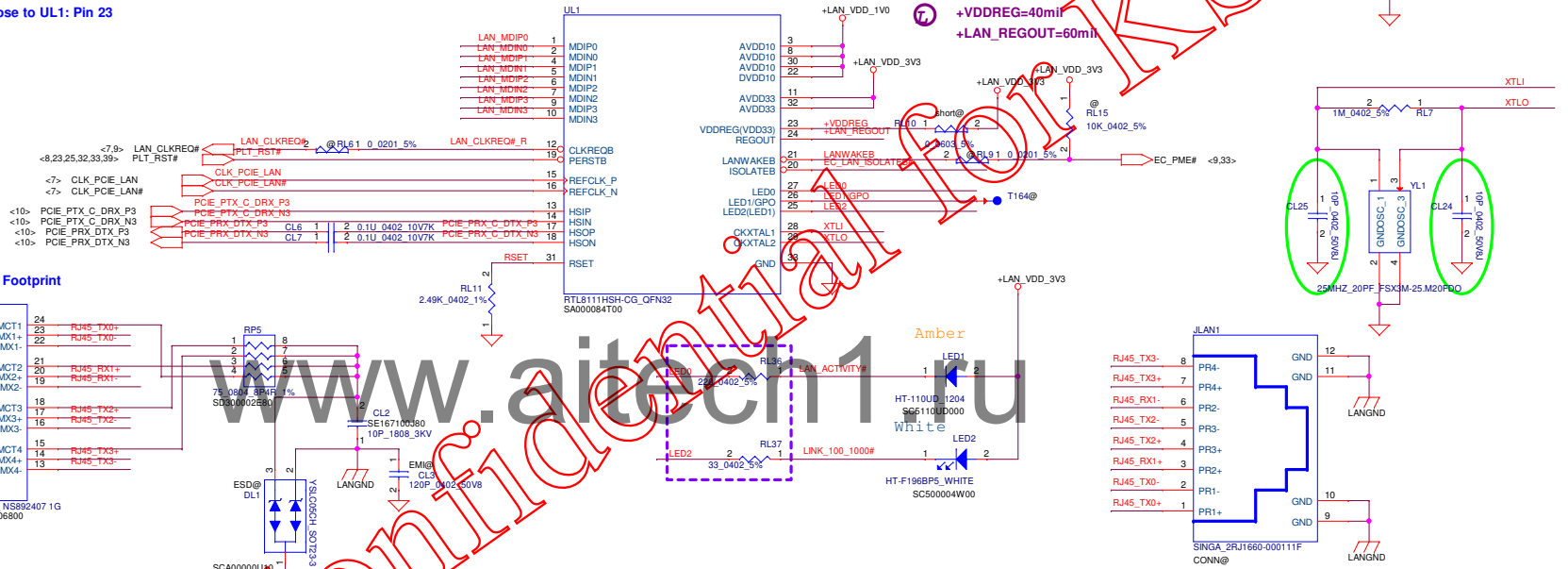
+LAN_VDD_3V3 Rising time
need >0.5mS and <100mS



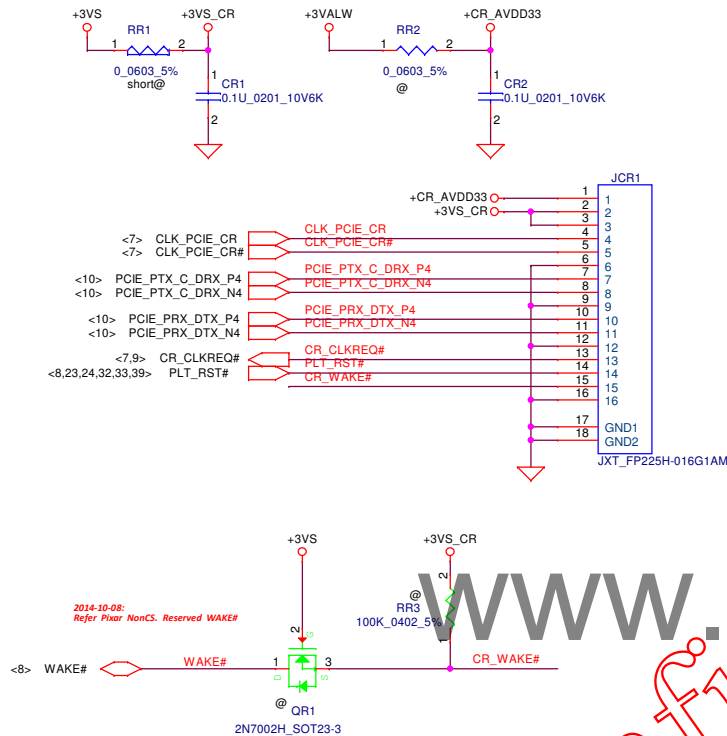
CL10& CL16 close to UL1: Pin 23



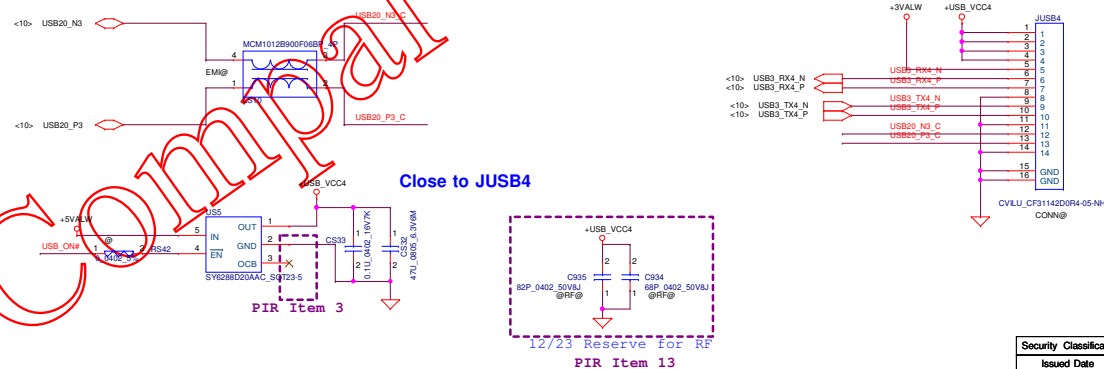
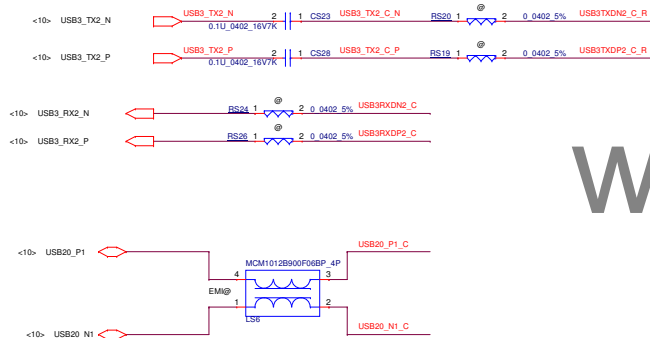
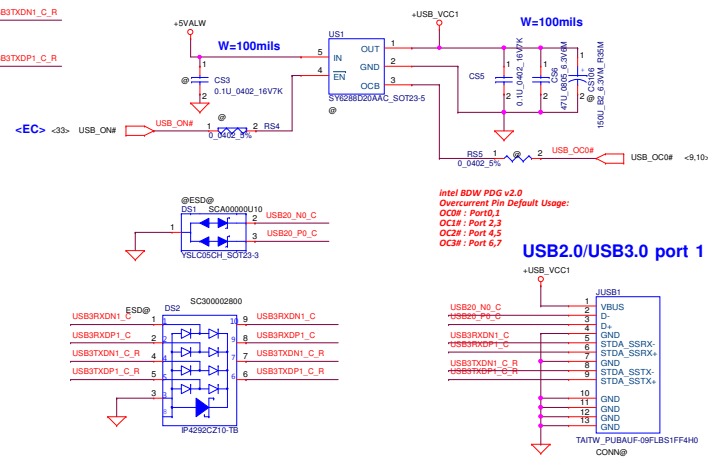
+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil



CardReader on Subboard

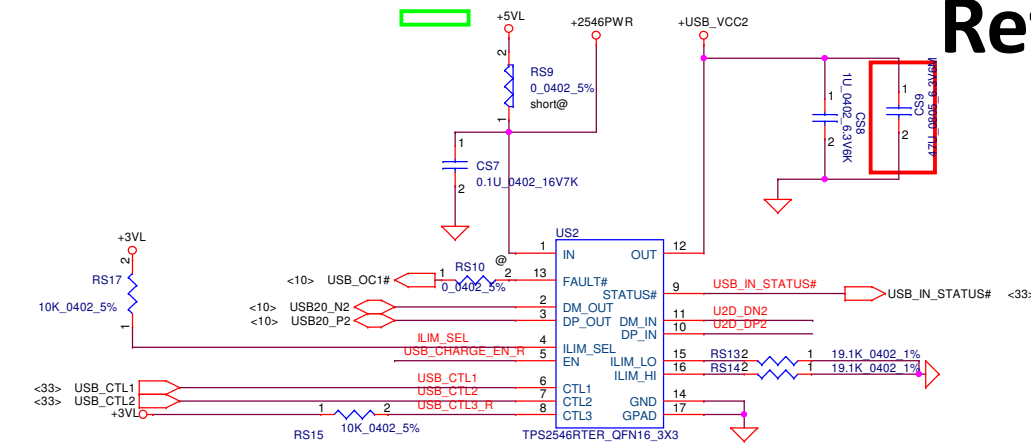


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				Size	Document Number	Rev
					LA-C501P	1.0
Date: Wednesday, April 22, 2015				Sheet	25	of 63



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Date: Wednesday, April 22, 2015			Sheet	26 of 63

Refer Pixar

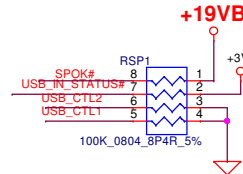
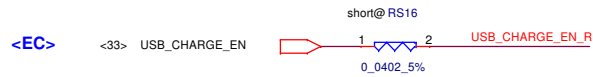


2014-10-13:Change Correct Power Net Name

$B+ \Rightarrow +19VB$

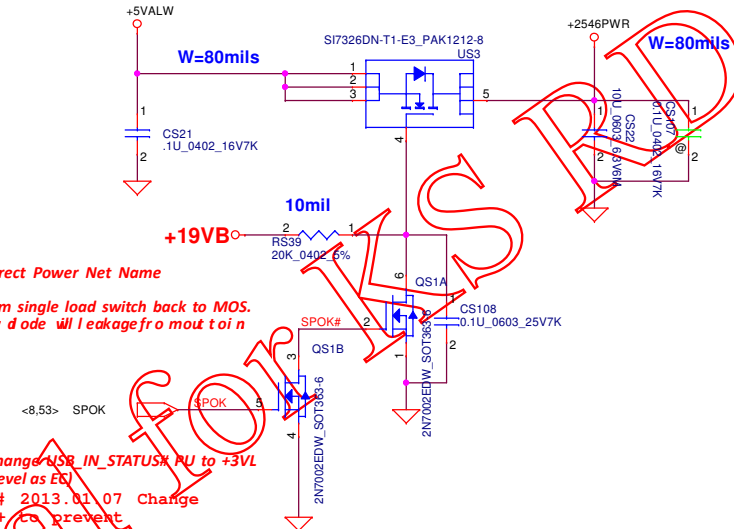
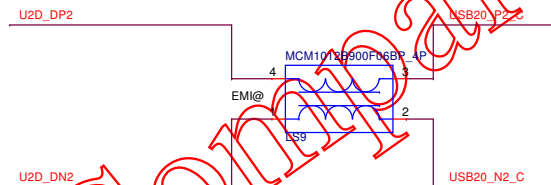
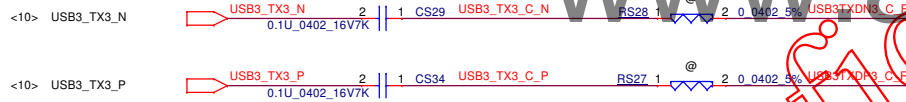
2014-10-21: Change from single load switch back to MOS.
Load Switch have body diode will leakage from output to in

2014-10-20: Change USB_IN_STATUS# PU to +3VL
(same power level as EC)

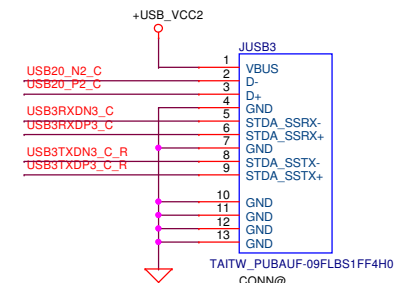
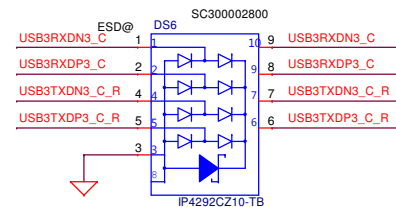


~~2014-10-20: Change USB_IN_STATUS# PU to +3VL
(same power level as EC)~~

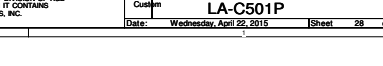
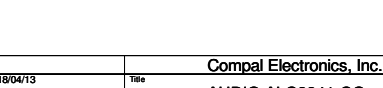
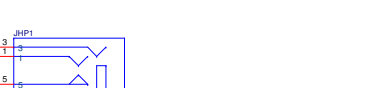
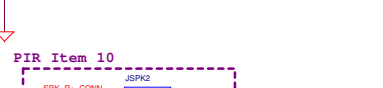
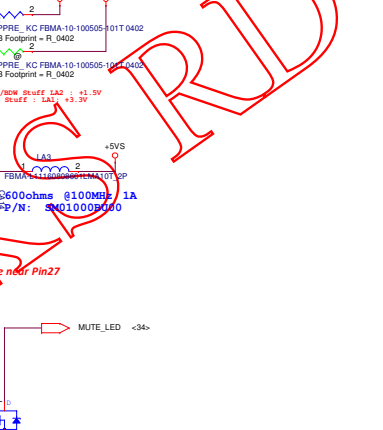
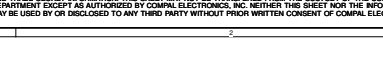
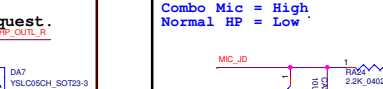
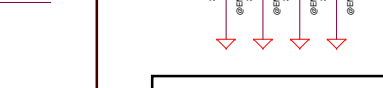
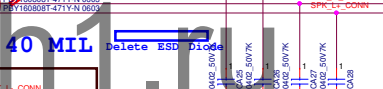
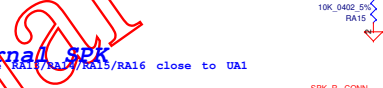
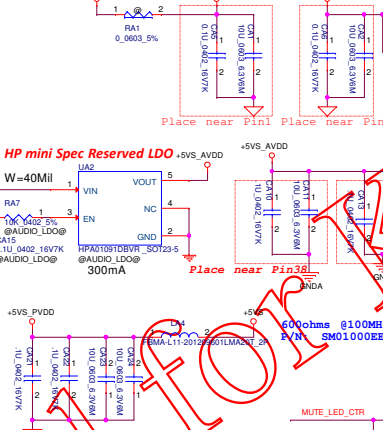
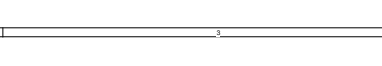
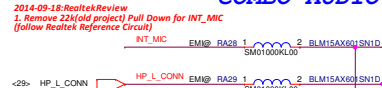
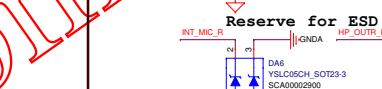
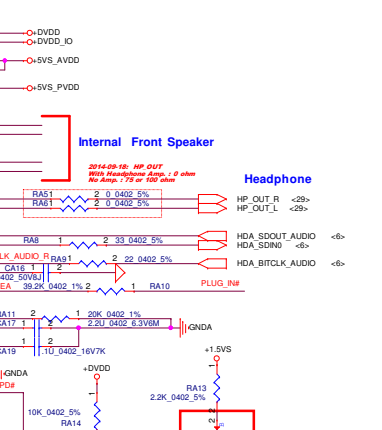
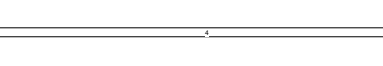
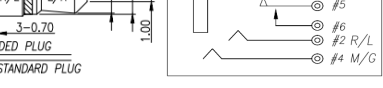
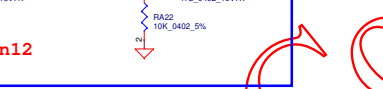
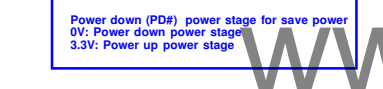
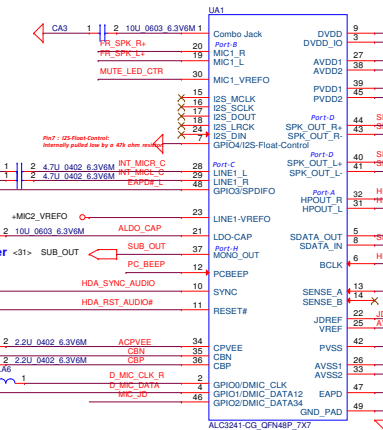
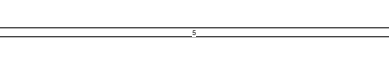
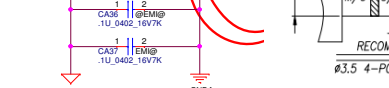
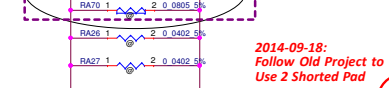
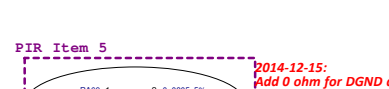
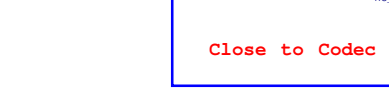
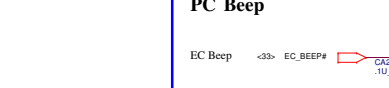
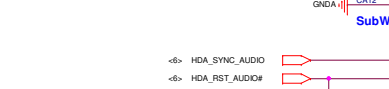
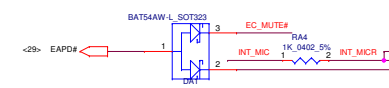
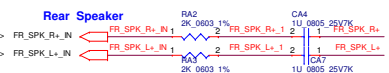
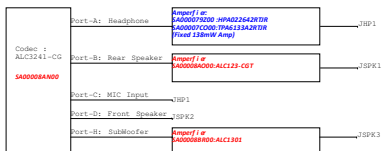
Pixar PV# 2013.01.07 Change
+VL to B+ to prevent
leakage



USB2.0/USB3.0 port 2



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				Custom	LA-C501P	
				Date: Wednesday, April 22, 2015		Sheet



Power down (PD#) power stage for save power
0V: Power down power stage
3.3V: Power up power stage

PC BEEP



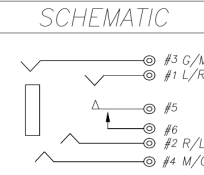
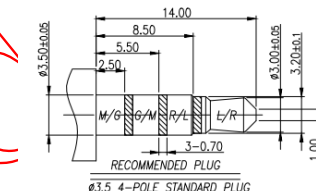
Close to Codec pin12

PIR Item 5

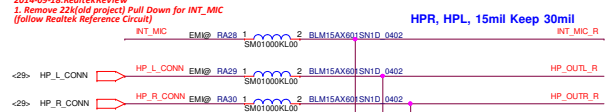


2014-12-15:
Add 0 ohm for DGND and AGND plane bridge by HP

2014-09-18:
Follow Old Project to Use 2 Shorted Pad



COMBO AUDIO JACK



HPR, HPL, 15mil Keep 30mil



2015 Cocoa Audio Design Requirements v1.2doc

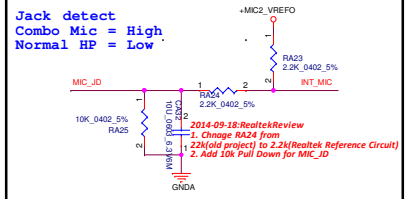
Combo jack pin configuration

Tip = Left

1st ring = Right

2nd ring = Ground

Sleeve = Mono microphone



Jack detect
Combo Mic = High
Normal HP = Low

2014-09-18: Realtek Review

1. Change RA24 from 2.2K (old project) to 2.2K (Realtek Reference Circuit)

2. Add 10K Pull Down for MIC_ID

2014-09-18: Realtek Review

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2014-09-18: Realtek Review

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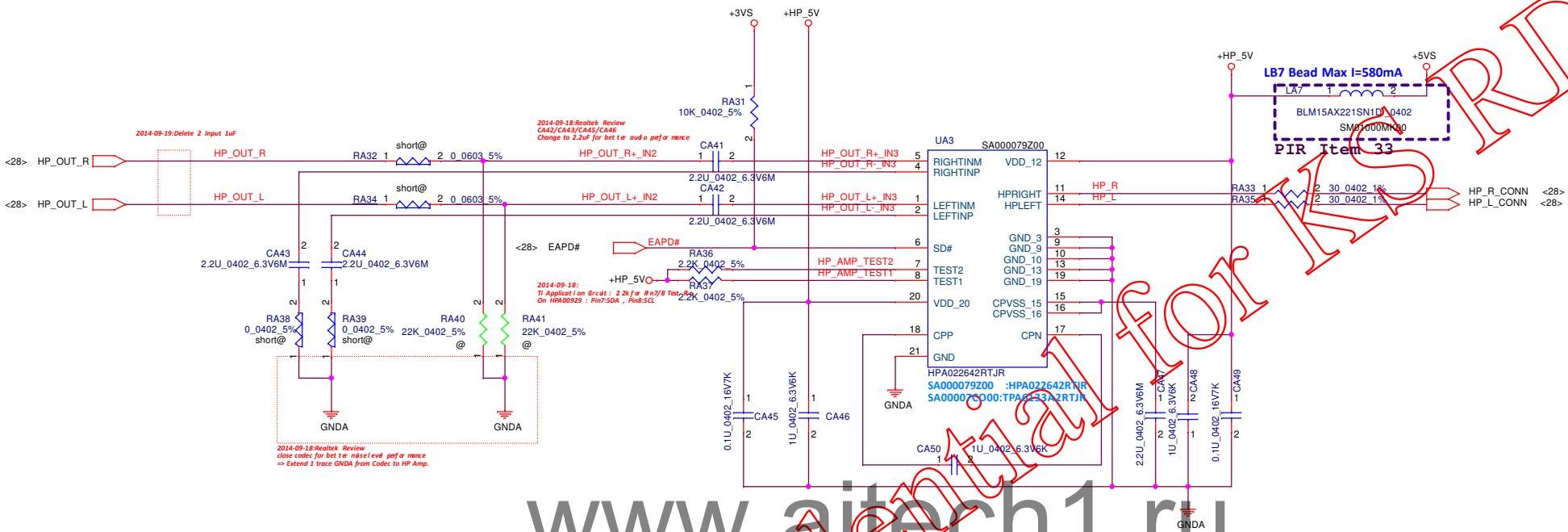
2. Add 10K Pull Down for MIC_ID

2014-09-18: Realtek Review

1. Change RA24 from 2.2K (old project) to 2.2K (Realtek Reference Circuit)

2. Add 10K Pull Down for MIC_ID

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Issued Date	2015/04/13	Deciphered Date	2015/04/13		Audio ALC3241-CG	
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Date: Wednesday, April 22, 2015						Sheet 28 of 83

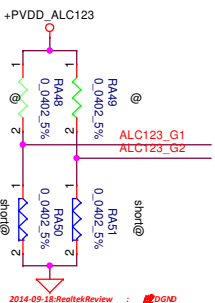
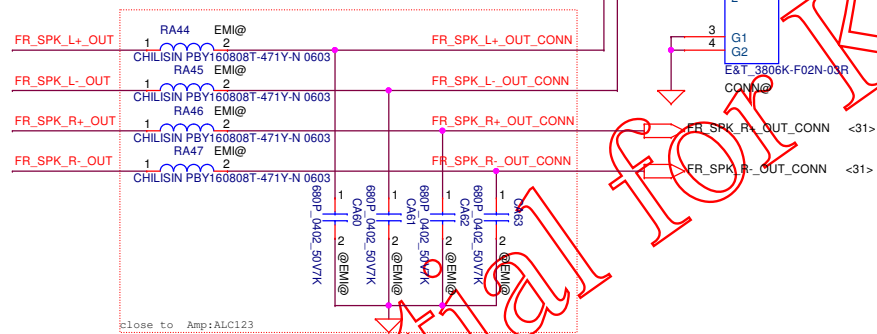
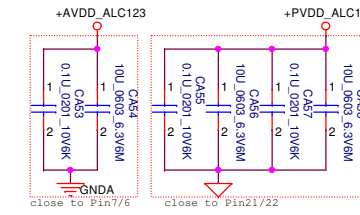
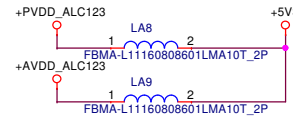
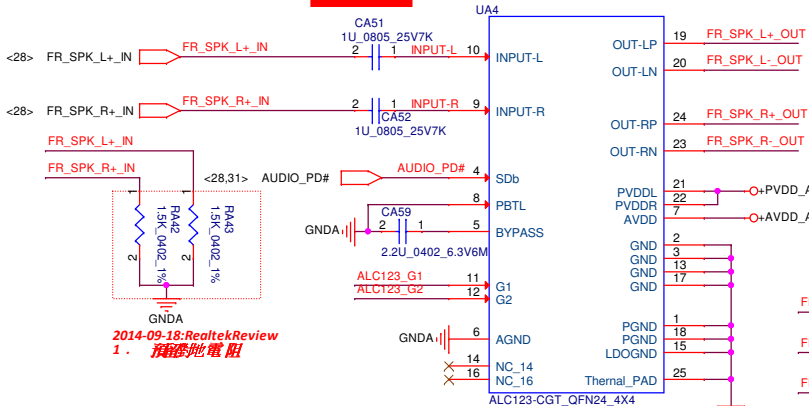


www.aitech1.ru

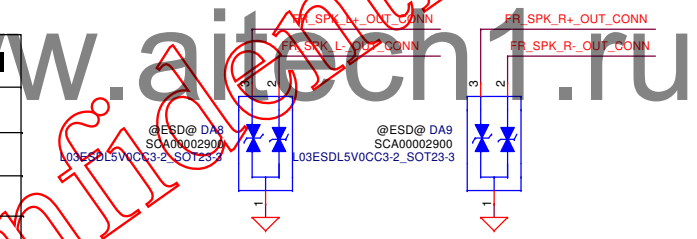
Compal Confidential

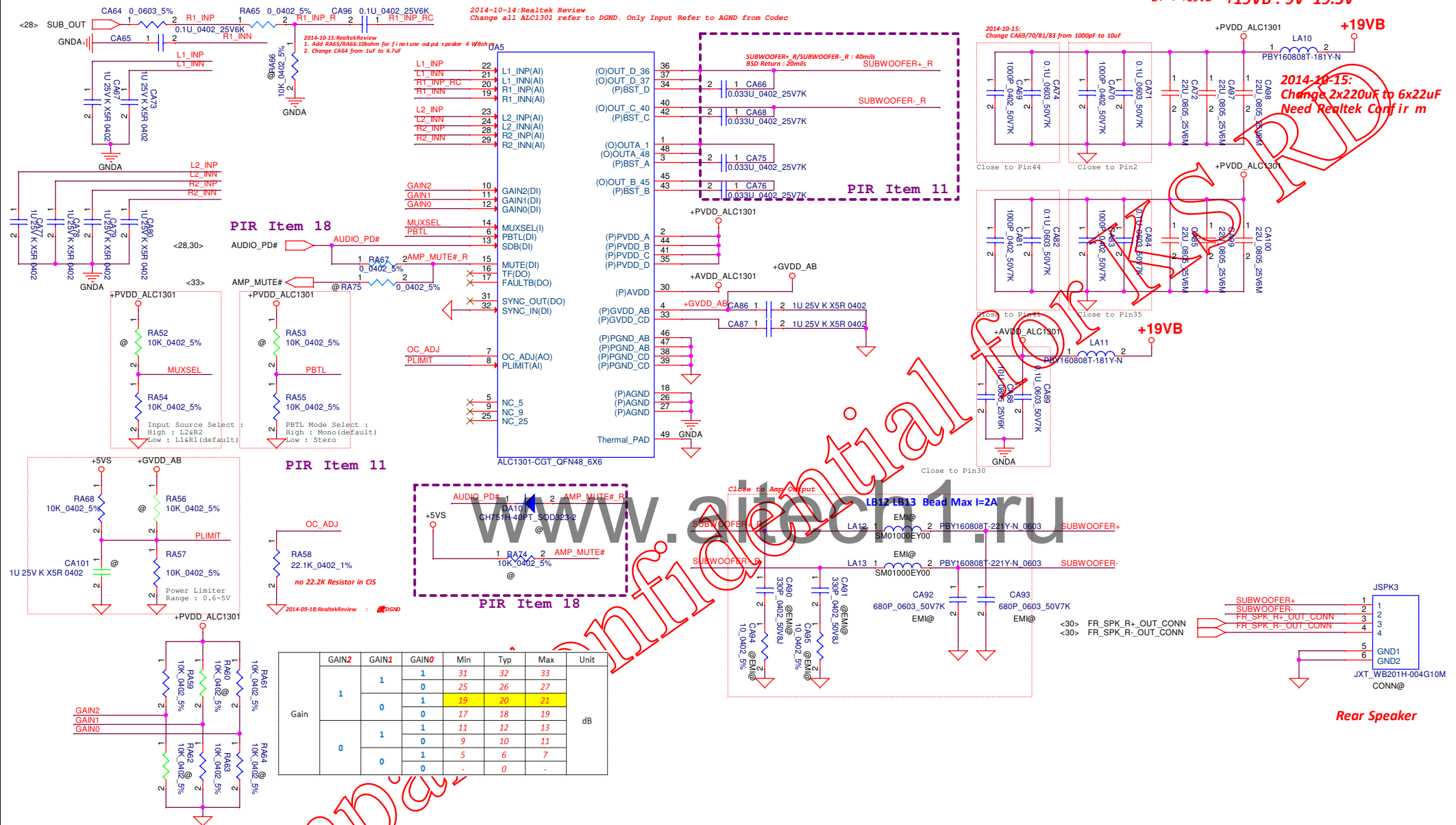
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/04/13	Deciphered Date	2018/04/13	Title	
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Date:	Wednesday, April 22, 2015	Sheet	29	of	63

2014-09-17:RealtekReview
1. 靠H端加隔離



G2	G1	Differential
0	0	11dB
0	1	14dB
1	0	19dB
1	1	24dB

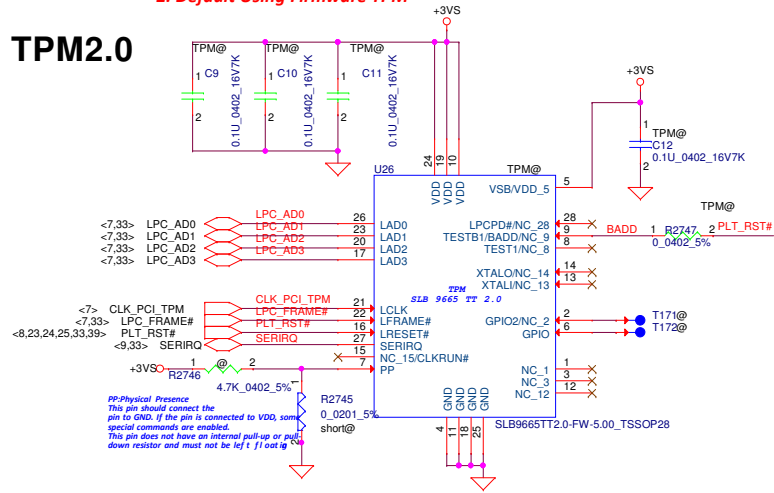




	GAIN2	GAIN1	GAIN0	Min	Typ	Max	Unit
Gain	1	1	1	31	32	33	dB
			0	25	26	27	
		0	1	19	20	21	
			0	17	18	19	
	0	1	1	11	12	13	
			0	9	10	11	
		0	1	5	6	7	
			0	-	0	-	

2014-10-14:
1. Updated Pin def i net o TP M0
2. Default Using Firmware TPM

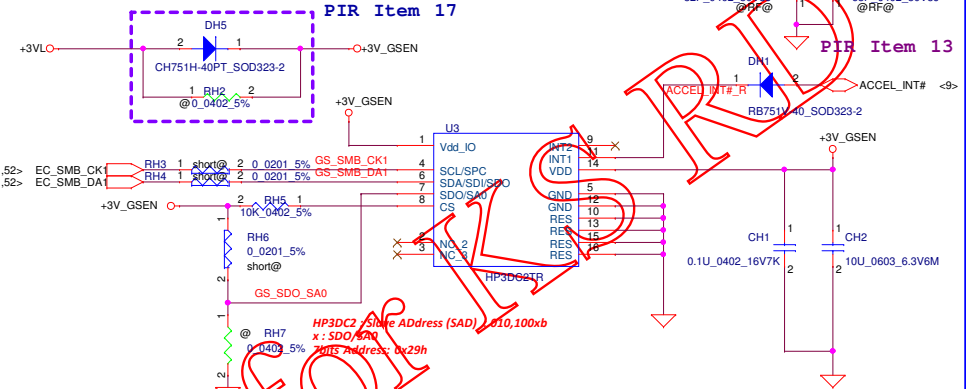
TPM2.0



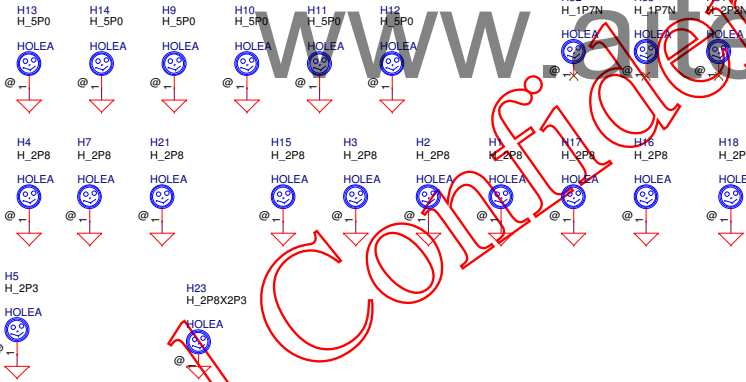
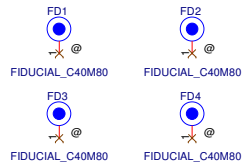
12/23 Reserve for RF

ACCELEROMETER

2014-10-14: Follow Phelps
1. Keep Power Rail +3VLW
2. Remove INT# PU RH2.
(ACCEL_INT# have PU 10K to +3V_PCH to PCH_GPIO46)
3. SCL/SDA Direct Connect to EC_SMBus.
EC_SMBus PU to +3VL



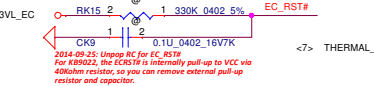
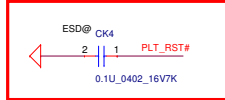
Screw Hole



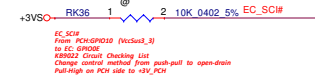
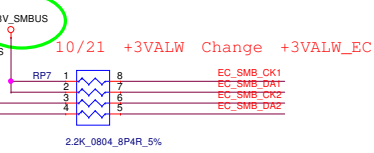
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						Size		Document Number		Rev	
								LA-C501P		1.0	
						Date:		Wednesday, April 22, 2015		Sheet 32 of 63	

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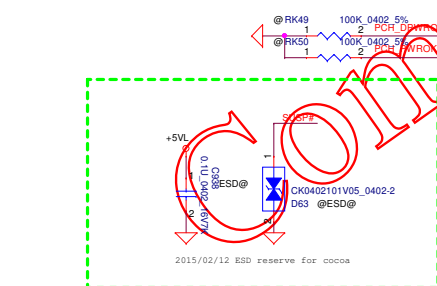
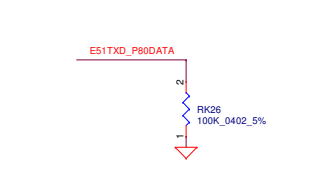
PV# 2013.01.29 Add CK4 for ESD protect i on



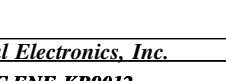
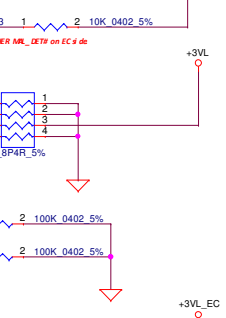
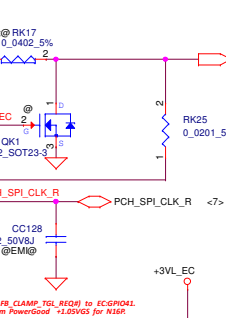
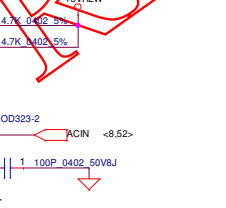
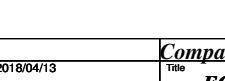
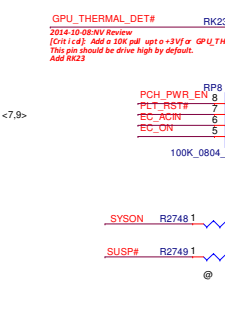
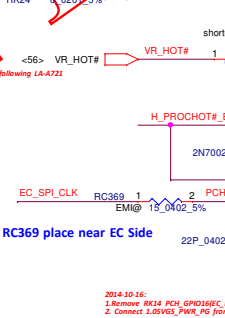
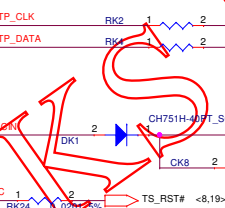
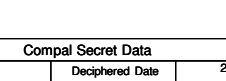
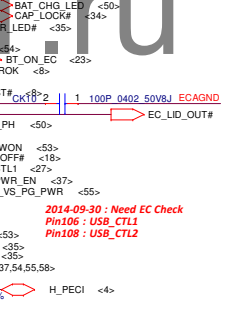
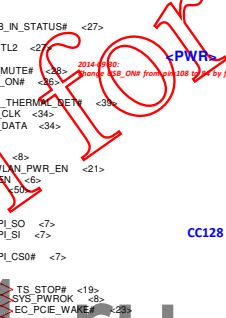
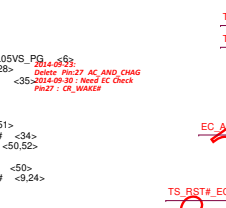
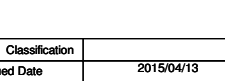
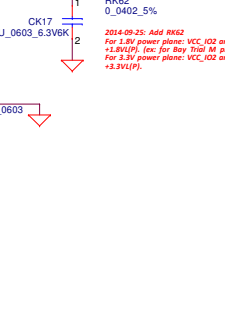
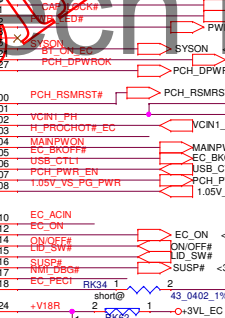
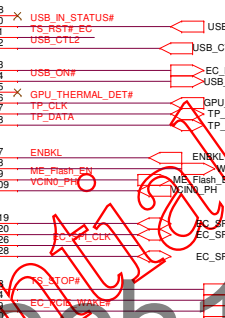
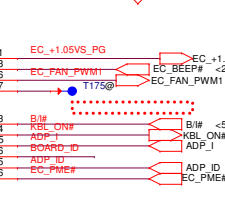
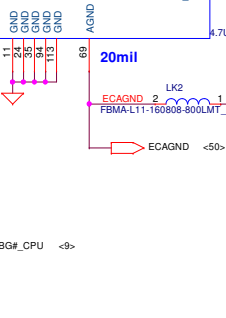
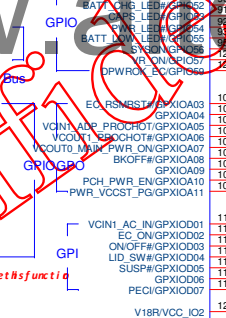
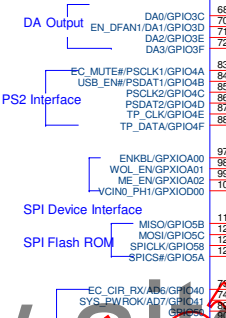
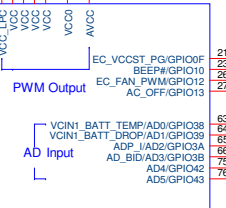
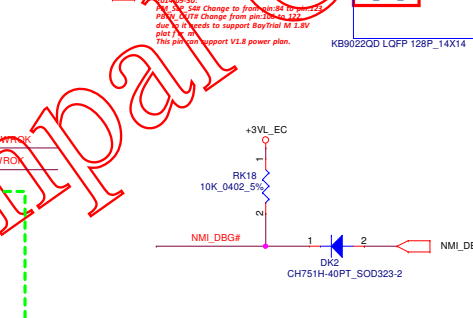
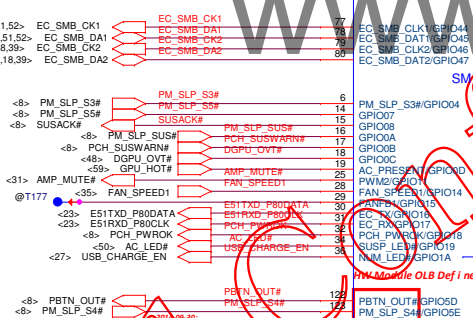
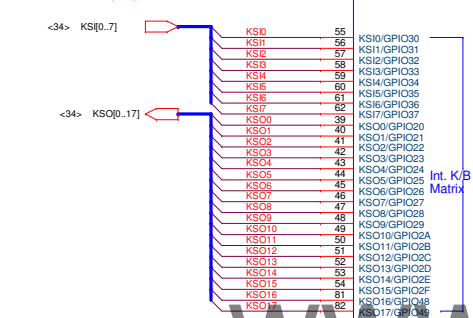
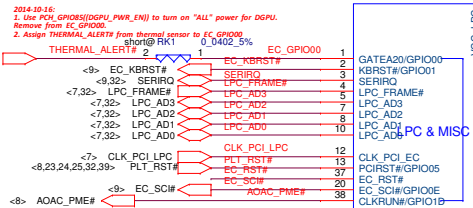
PIR Item 12



PIR Item 11



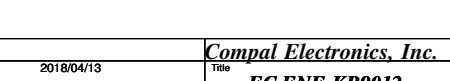
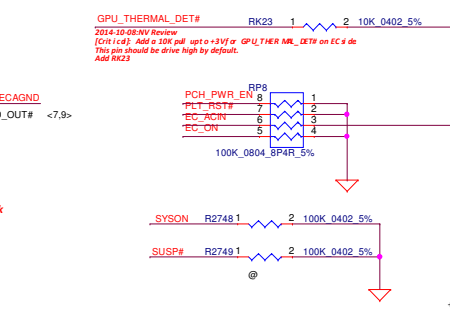
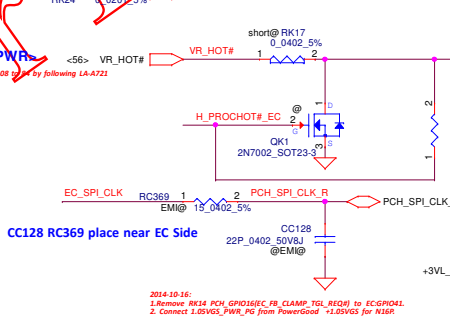
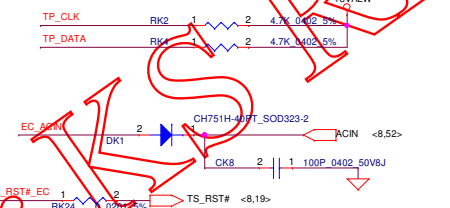
2015/02/12 RSD reserve for cocoa



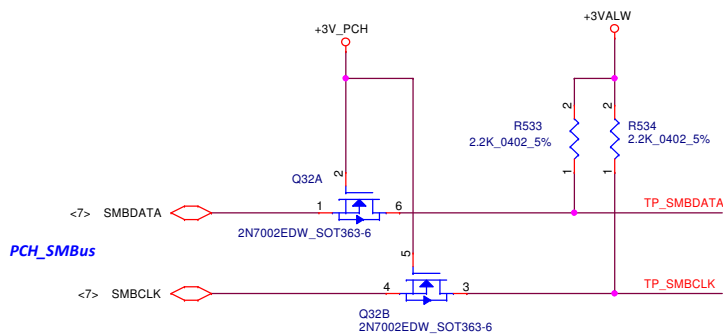
Board ID control for 15

UMA	DB	SI	PV	MV
RK13	0 ohm	15K ohm	27K ohm	43K ohm
DIS	12k ohm	20k ohm	33k ohm	47k ohm
RK13				

Board ID control

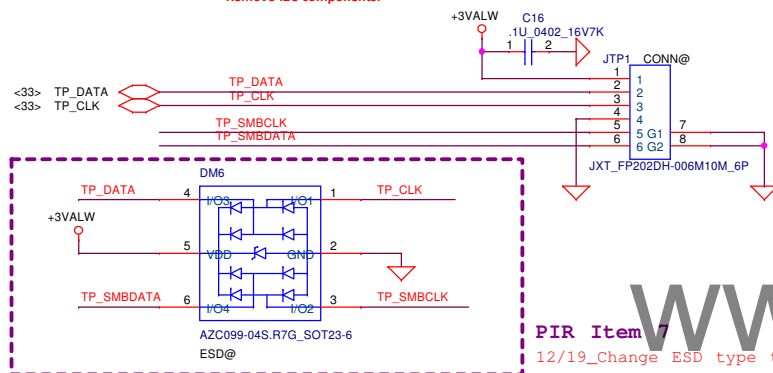


Touch pad conn

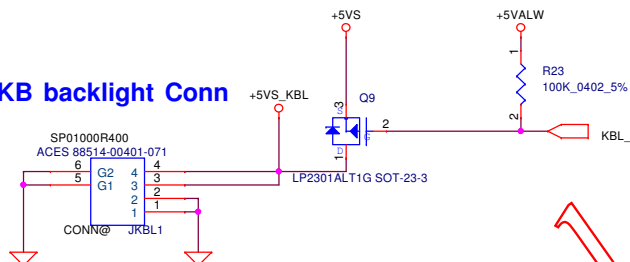


2014-10-14:
Confirm with Synaptics "Only" PS2+ SMBus interface
Remove I2C components.

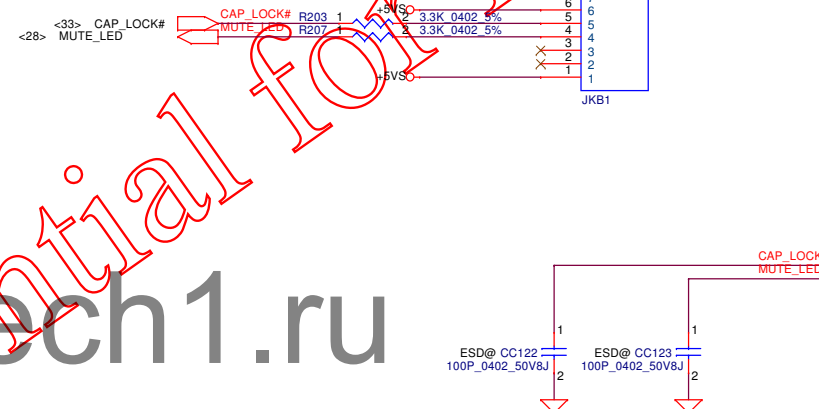
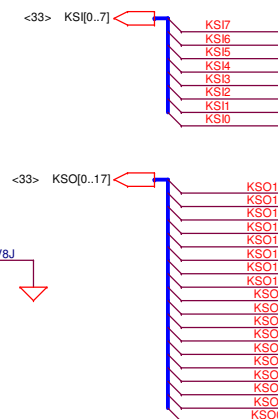
EC PS2



KB backlight Conn

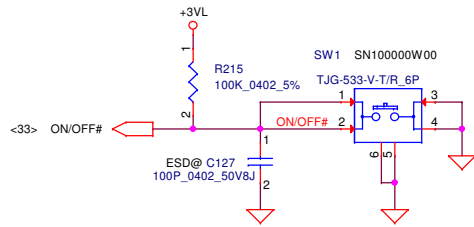


Keyboard conn

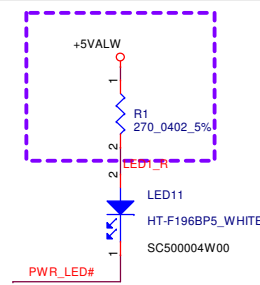
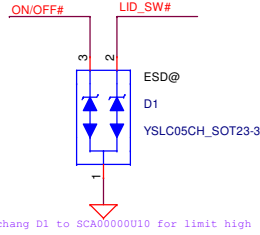


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Size		Document Number		Rev	
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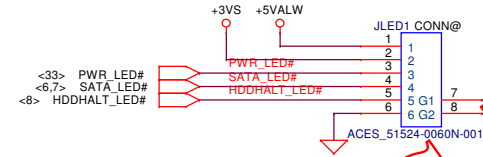
Power Button Switch



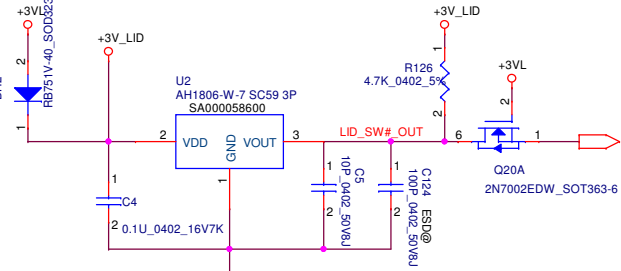
ESD Diode



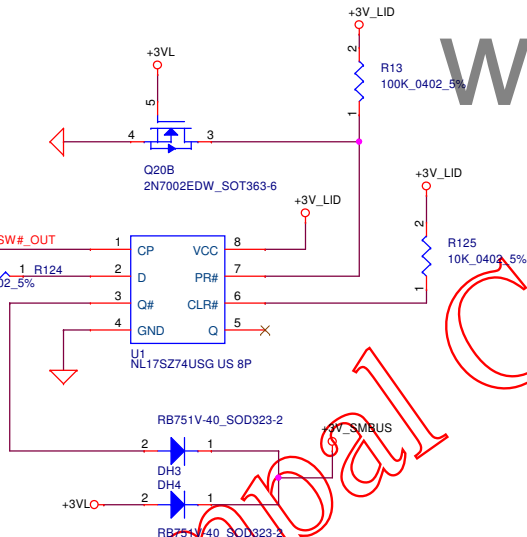
to LED Board



Lid Switch (Hall Effect Sensor)

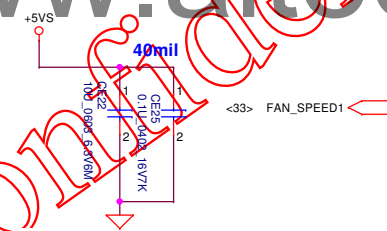


PIR Item 12



FAN conn

2014-09-26:
Change to PWM Fan. Remove Fan Driver APE633M



TRUTH TABLE

Inputs				Outputs		Operating Mode
PR	CLR	CP	D	Q	Q	
L	H	X	X	L	L	Asynchronous Set
H	L	X	X	H	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	h	L	L	Load and Read Register
H	H	↑	h	L	L	Load and Read Register
H	H	↑	X	NC	NC	Hold

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
↑ = Low-to-High Transition
↓ = Not a Low-to-High Transition

For I_{CC} reasons, DO NOT FLOAT inputs

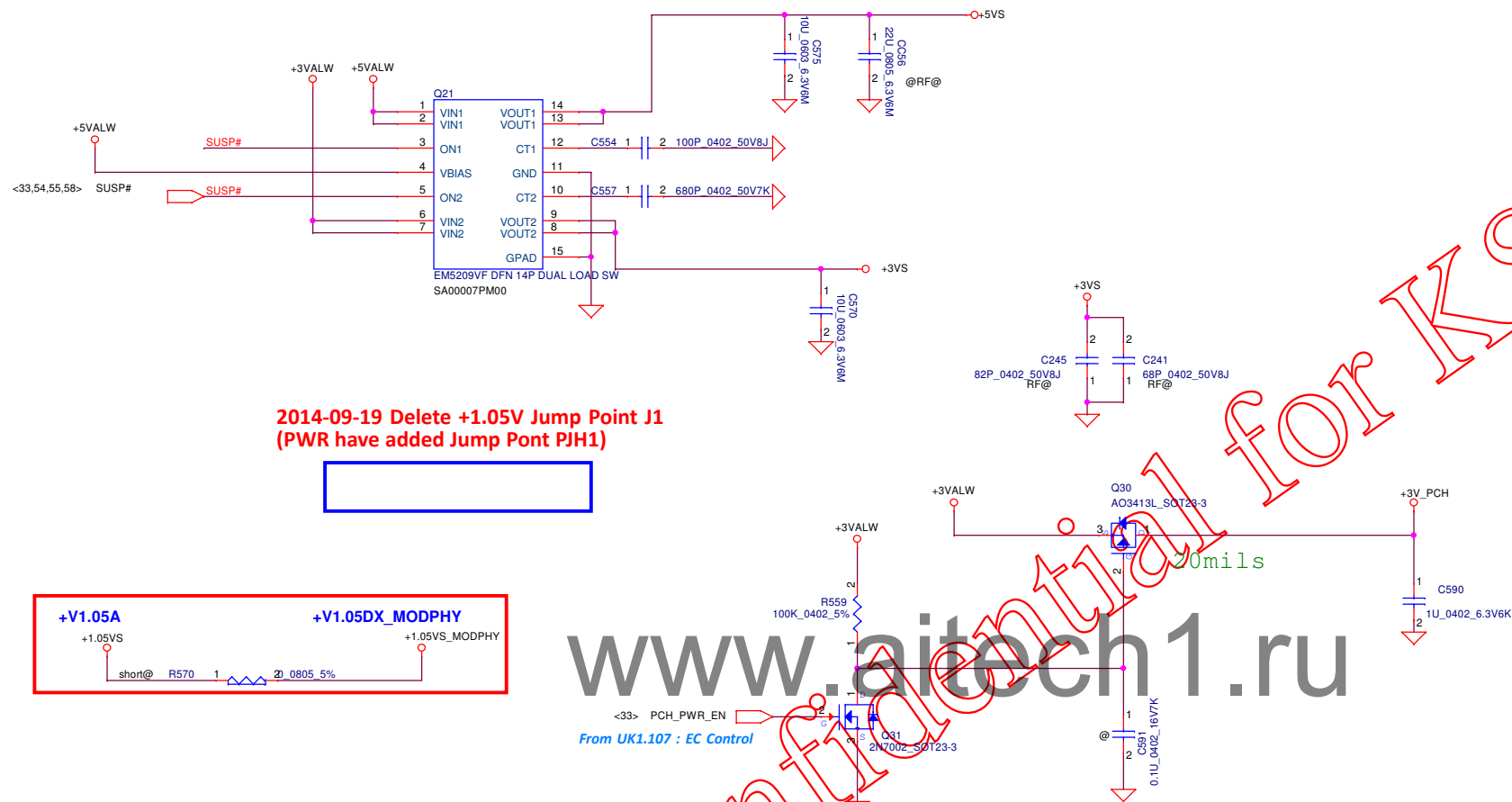
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Reserve for HW

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				Rev	1.0



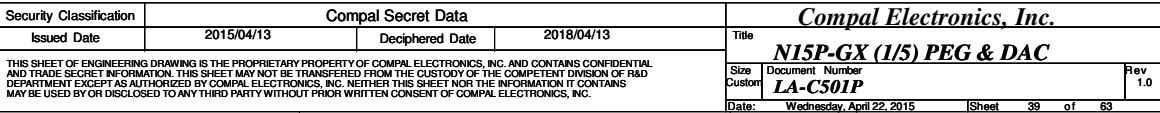
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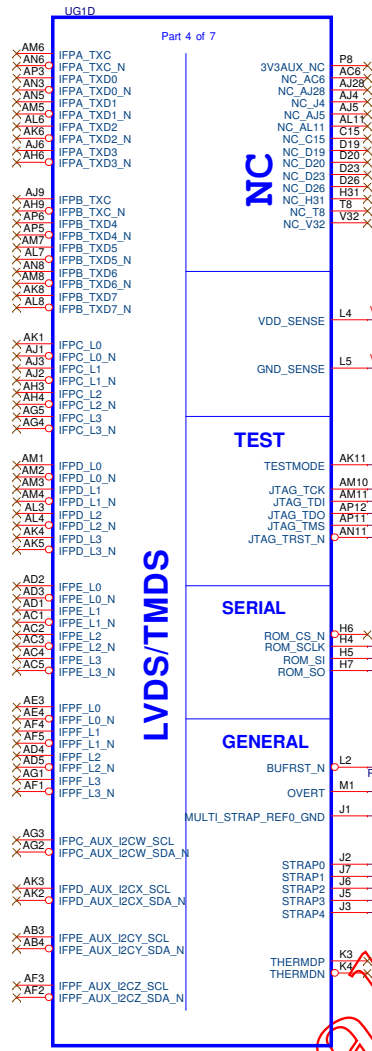
Reserve for HW

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				Document Number	
				LA-C501P	
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trace width: 16mils
differential voltage sensing.
differential signal routing.

RG10/RG11 put it close
to power supply.

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS_MAIN	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SO	+3VGS_MAIN	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	+3VGS_MAIN	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep pull-up to 3V3_AON and pull-down to GND foot print and stuff 50K ohm pull-up				
STRAP1					
STRAP2					
STRAP3					
STRAP4					

SKU	Device ID	bit5 to bit0
N16P-GT		

Resistor Values	Pull-up to +3VGS_MAIN	Pull-down to Gnd
5K	1000 =8	0000 =0
10K	1001 =9	0001 =1
15K	1010 =A	0010 =2
20K	1011 =B	0011 =3
25K	1100 =C	0100 =4
30K	1101 =D	0101 =5
35K	1110 =E	0110 =6
45K	1111 =F	0111 =7

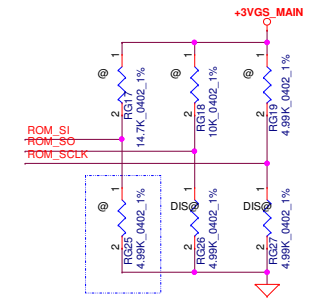
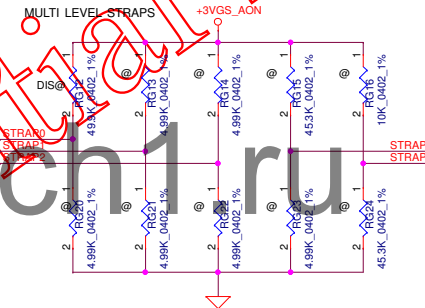


Table 6. N16P-GT DDR3L Recommended Memories

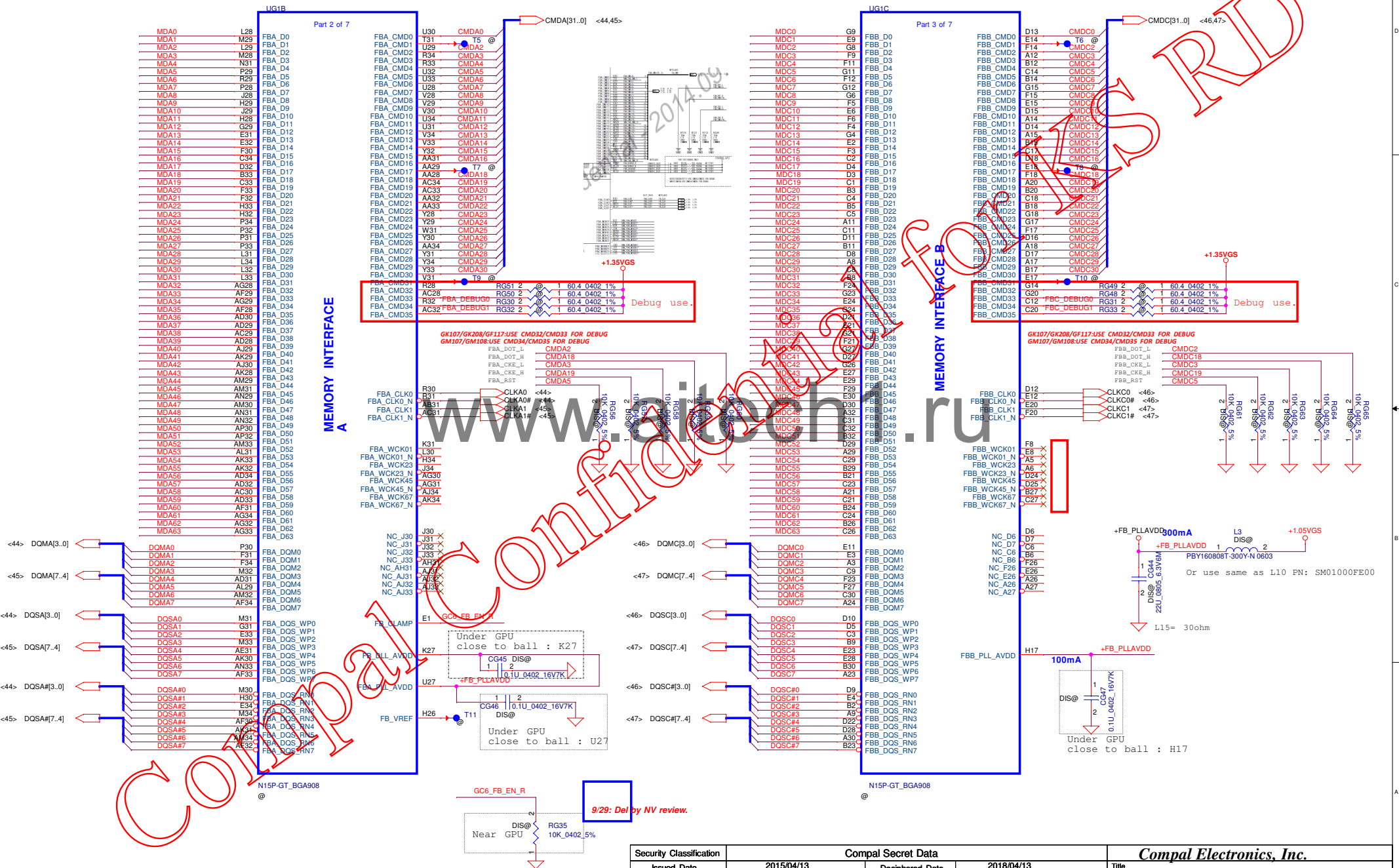
Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed (MHz)	Memory Date Code (Minimum)	Memory Status
DDR3L	1.35V/ 1.35V	128Mx16	Single Rank	Hynix	H5TC26A3FFR-11C	F-die	0x9	900	N/A	Production candidate
				Microton	MT41J28M16JT-093G-K	K-die	0xA	900	1322	Production candidate
				Samsung	K4V72G16A0Q-BC1A	Q-die	0xB	900	N/A	Production candidate
		256Mx16	Single Rank	Hynix	H5TC46A3AFR-11C	A-die	0x3	900	N/A	Production candidate
				Microton	MT41J256M16HA-093G-E	E-die	0x4	900	1322	Production candidate
				Samsung	K4H14G16A0D-BC1A	D-die	0x5	900	N/A	Production candidate



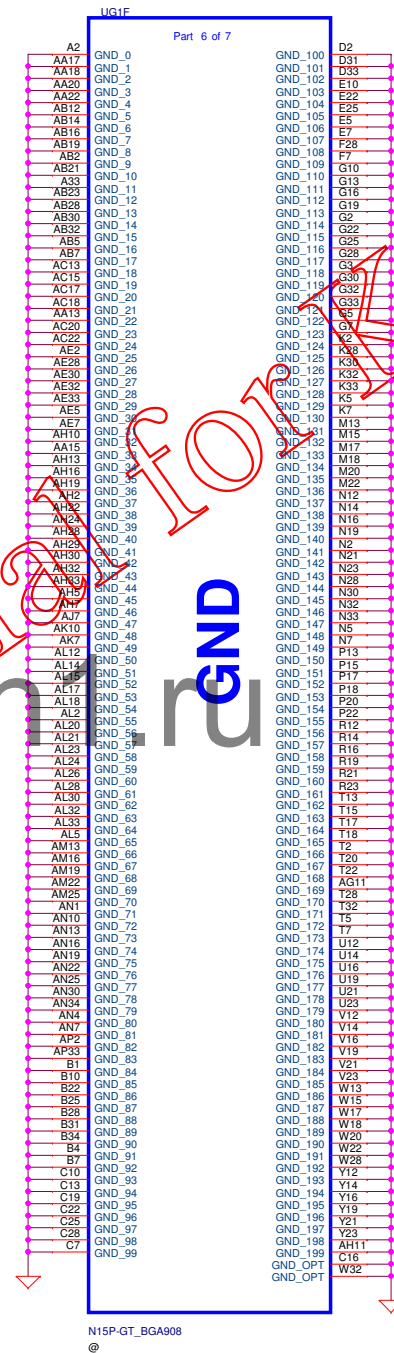
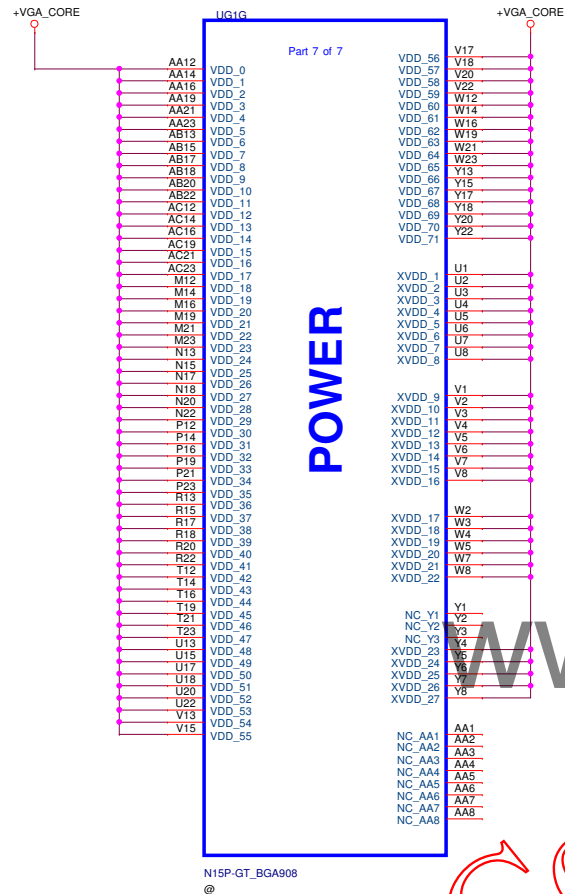
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					Size Custom	Document Number	Rev
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<44> MDA[15..0] MDA[15..0]
<44> MDA[31..16] MDA[31..16]
<45> MDA[47..32] MDA[47..32]
<45> MDA[63..48] MDA[63..48]

<46> MDC[15..0] MDC[15..0]
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<47> MDC[47..32] MDC[47..32]
<47> MDC[63..48] MDC[63..48]

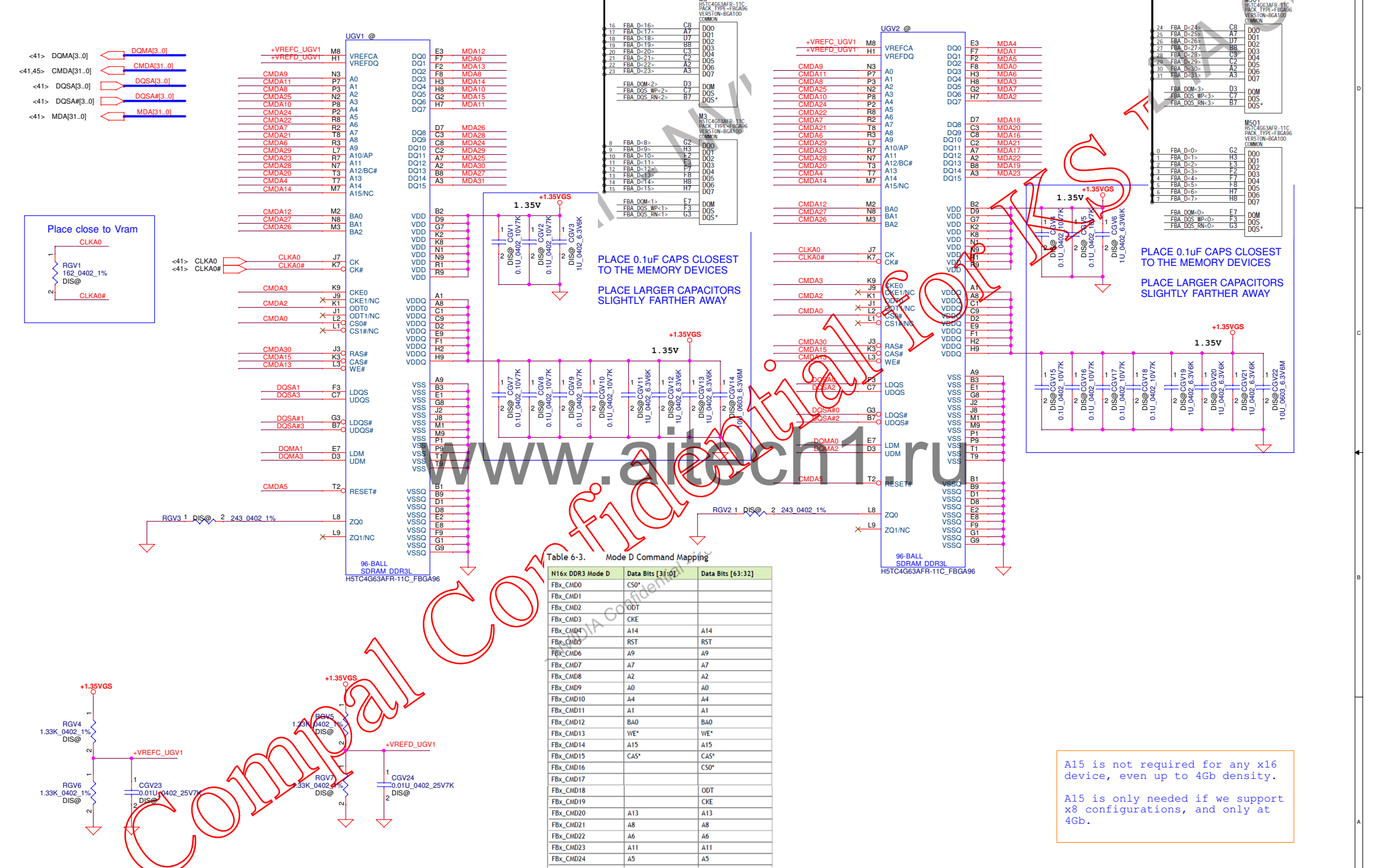


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Title			
N15P-GX (3/5) TMDs/LVDS			
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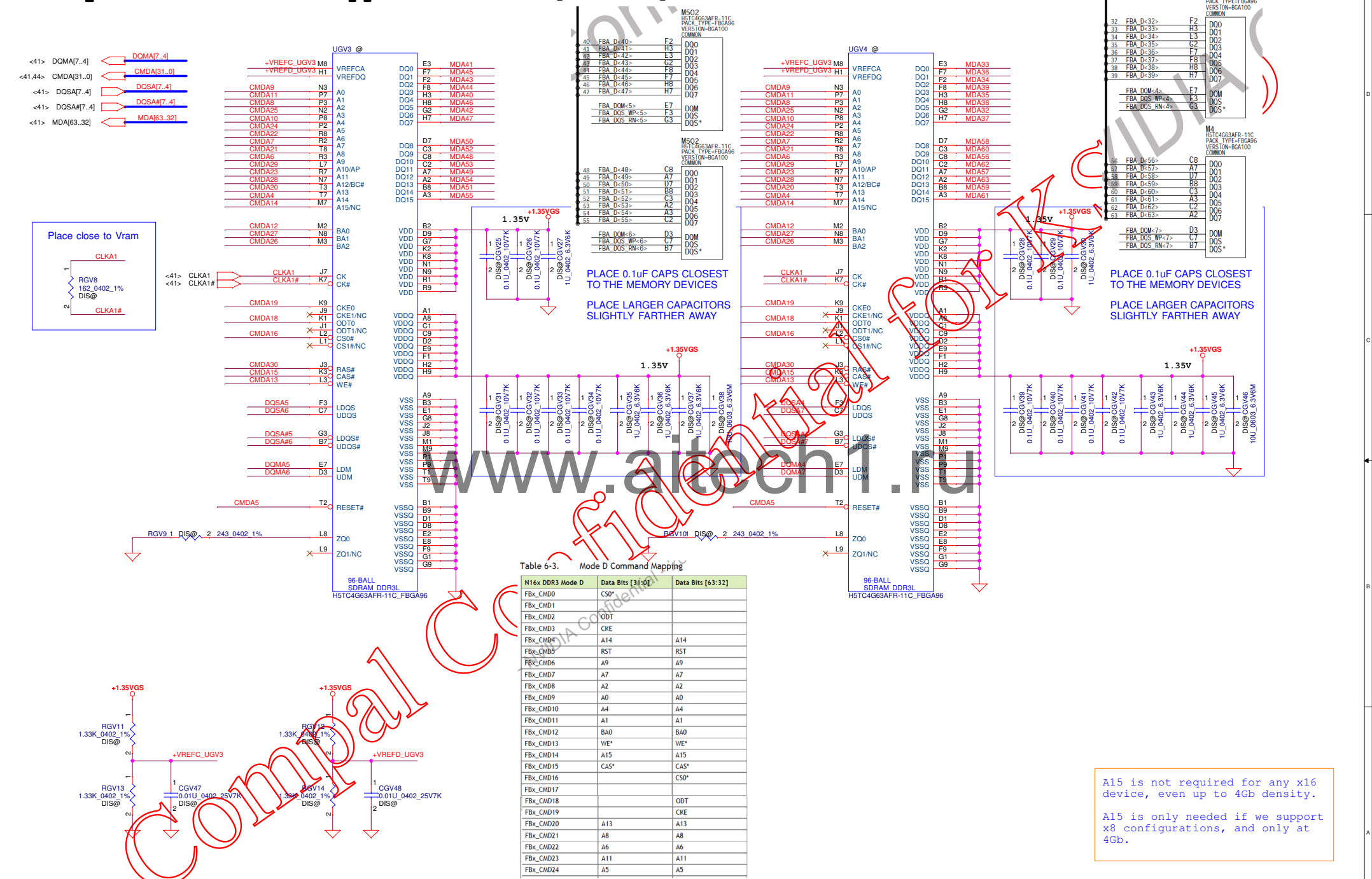
Memory Partition A - Lower 32 bits [31..0]



A15 is not required for any x16 device, even up to 4Gb density.

A15 is only needed if we support x8 configurations, and only at 4Gb.

Memory Partition A - Upper 32 bits [63..32]

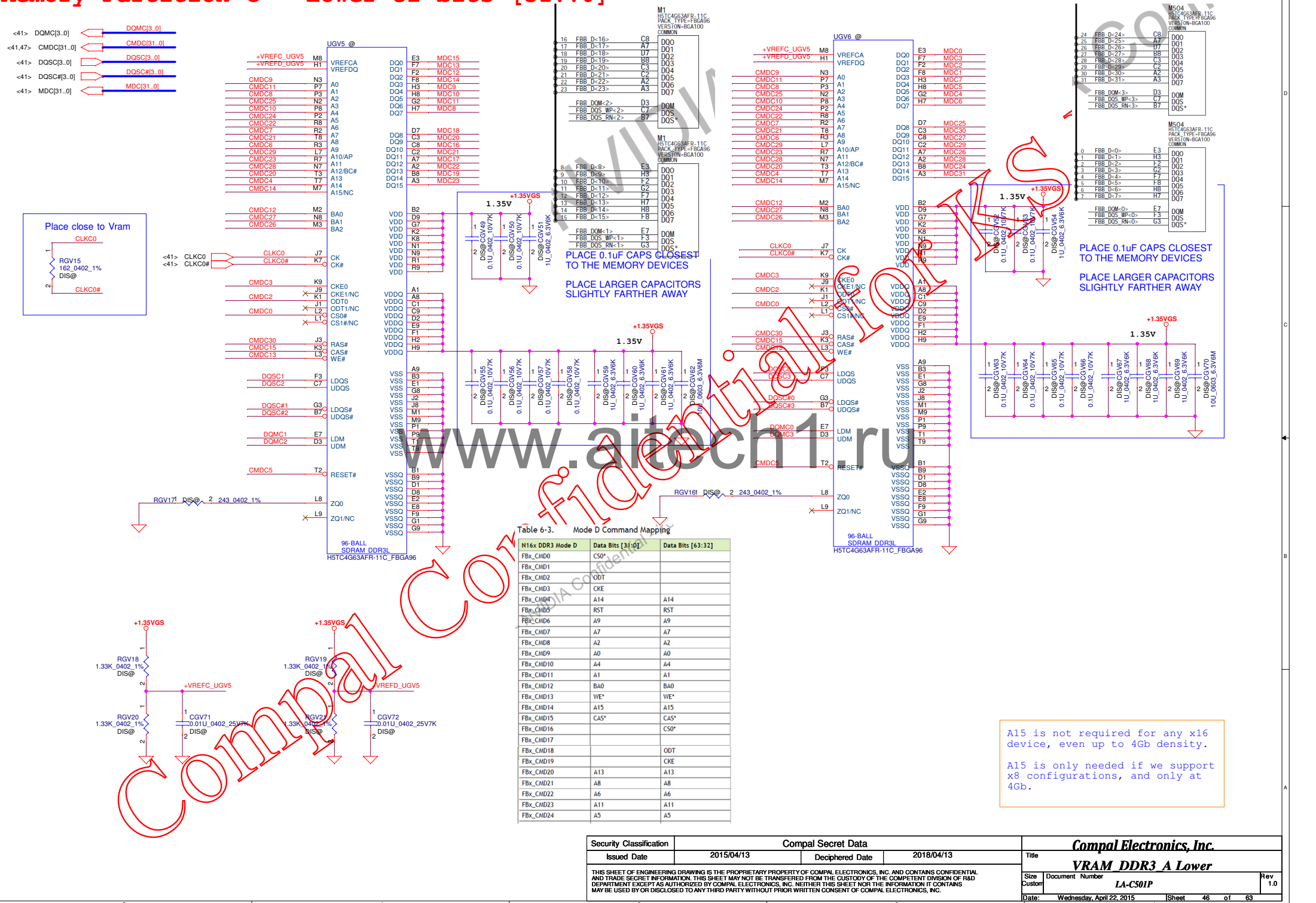


N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FbX_CMD0	CS0*	
FbX_CMD1		
FbX_CMD2	ODT	
FbX_CMD3	CKE	
FbX_CMD4	A14	A14
FbX_CMD5	RST	RST
FbX_CMD6	A9	A9
FbX_CMD7	A7	A7
FbX_CMD8	A2	A2
FbX_CMD9	A0	A0
FbX_CMD10	A4	A4
FbX_CMD11	A1	A1
FbX_CMD12	BA0	BA0
FbX_CMD13	WE*	WE*
FbX_CMD14	A15	A15
FbX_CMD15	CAS*	CAS*
FbX_CMD16		CS0*
FbX_CMD17		
FbX_CMD18		ODT
FbX_CMD19		CKE
FbX_CMD20	A13	A13
FbX_CMD21	A8	A8
FbX_CMD22	A6	A6
FbX_CMD23	A11	A11
FbX_CMD24	A5	A5

Al5 is not required for any x16 device, even up to 4Gb density.

Al5 is only needed if we support x8 configurations, and only at 4Gb.

Memory Partition C - Lower 32 bits [31..0]



A15 is not required for any x16 device, even up to 4Gb density.
A15 is only needed if we support x8 configurations, and only at 4Gb.

Memory Partition C - Upper 32 bits [63..32]

<41> DQMC[7..4] → DQMC[7..4]
 <41,46> CMD[31..0] → CMD[31..0]
 <41> DQSC[7..4] → DQSC[7..4]
 <41> DQSC[7..4] → DQSC[7..4]
 <41> MDC[63..32] → MDC[63..32]

UGV7 @
 VREFCA VREFDQ
 CMD09 N3
 CMD11 P7
 CMD05 P3
 CMD25 N2
 CMD24 P2
 CMD22 R8
 CMD07 R2
 CMD21 T8
 CMD06 R3
 CMD29 L7
 CMD23 R7
 CMD28 N7
 CMD20 T3
 CMD14 T7
 M7
 A10/AP
 A12/BC#
 A15/NC

CLKC1
 CLKC1#
 CK
 CK#

CMD19 K9
 CMD18 X J9
 CMD16 X J1
 LT
 CS0#
 CS1#
 RAS#
 CAS#
 WE#

DQSC5 F3
 DQSC6 C7
 DQSC5 G3
 DQSC6 B7
 DQMC5 E7
 DQMC6 D3

RESET#
 ZQ0
 ZQ1/NC
 96-BALL SDRAM DDR3L
 HSTC4G63AFR-11C_FBG96

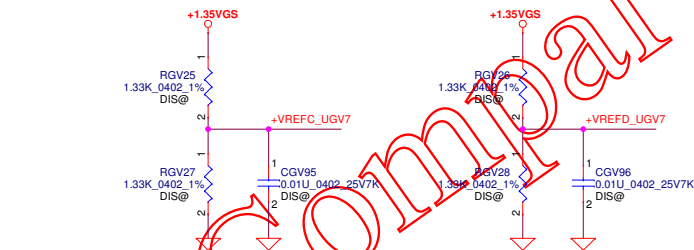


Table 6-3. Mode D Command Mapping

H16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FbxCMD0	CS0*	
FbxCMD1		
FbxCMD2	ODT	
FbxCMD3	CKE	
FbxCMD4	A14	A14
FbxCMD5	RST	RST
FbxCMD6	A9	A9
FbxCMD7	A7	A7
FbxCMD8	A2	A2
FbxCMD9	A0	A0
FbxCMD10	A4	A4
FbxCMD11	A1	A1
FbxCMD12	BA0	BA0
FbxCMD13	WE*	WE*
FbxCMD14	A15	A15
FbxCMD15	CAS*	CAS*
FbxCMD16	CS0*	CS0*
FbxCMD17		
FbxCMD18	ODT	
FbxCMD19	CKE	
FbxCMD20	A13	A13
FbxCMD21	A8	A8
FbxCMD22	A6	A6
FbxCMD23	A11	A11
FbxCMD24	A5	A5

PLACE 0.1uF CAPS CLOSEST TO THE MEMORY DEVICES
 PLACE LARGER CAPACITORS SLIGHTLY FARTHER AWAY

PLACE 0.1uF CAPS CLOSEST TO THE MEMORY DEVICES
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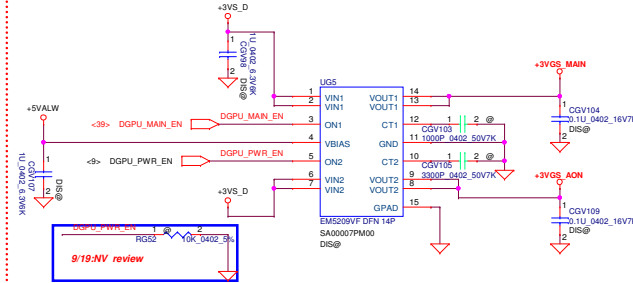
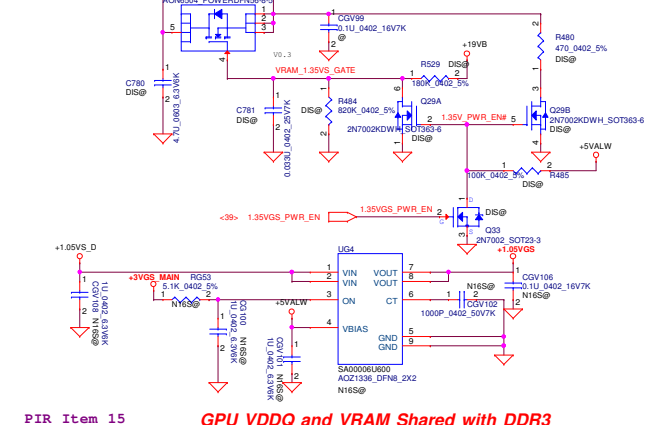
PLACE 0.1uF CAPS CLOSEST TO THE MEMORY DEVICES
 PLACE LARGER CAPACITORS SLIGHTLY FARTHER AWAY

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PLACE 0.1uF CAPS CLOSEST TO THE MEMORY DEVICES
 PLACE LARGER CAPACITORS SLIGHTLY FARTHER AWAY

A15 is not required for any x16 device, even up to 4Gb density.
 A15 is only needed if we support x8 configurations, and only at 4Gb.

919:NV add delay.



Power sequencing guidelines are provided relative to the ramping up of the main 3.3V system rail, which is the 3.3V input to the GPU.

The following condition is recommended:

3.3V \rightarrow NVVDD/PEX VDD \rightarrow FBVDD/Q

- ▶ All GPU power rails must ramp up after 3.3V.
- ▶ FBVDD/Q should ramp up after both NVVDD and PEX_VDD are in regulation.

All other 3.3V power rails can ramp up with 3.3V, and all other 1.05V power rails can ramp up with PEX_VDD. Figure 3-6 shows an example of proper GPU power up sequence.

IPPx_VDD powered at 3.3V can ramp up with other 3.3V power rails. IFPy_VDD powered at 1.05V can ramp up with other 1.05V power rails. Figure 3-7 shows an example of proper GPU power up sequence.

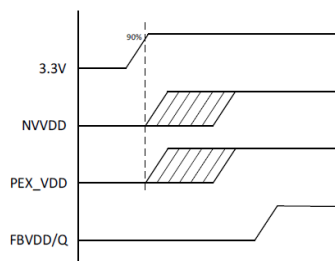


Figure 3-7. Example of Power-Up Sequencing Order

- 3.3V includes all rails powered at 3.3V; PEX_VDD includes all rails that are shared on 1.05V
- The ramp time for any rail must be more than 40 μ s and is recommended to be less than 2ms.
- Designs that support GC6 2.0 are required to meet all GC6 timing requirements.
- Refer to Section 18.2.3.2 for requirement details.
- PEX_VDD can ramp up before, after, or at the same time with HVDD.**
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped.
- Refer to the JEDEC Memory Specification for memory related power sequencing

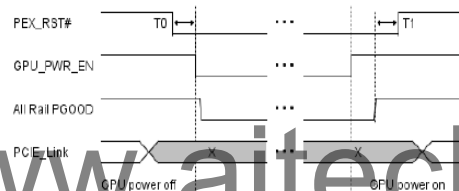


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

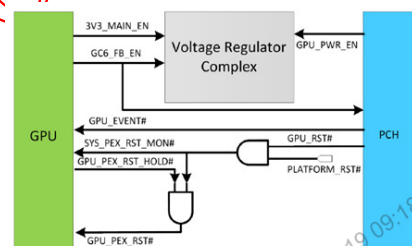
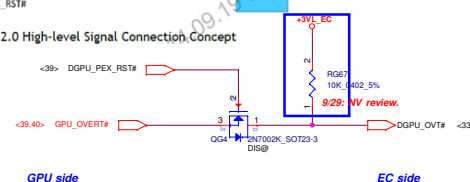


Figure 18-9. GC6 2.0 High-level Signal Connection Concept



The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 entry and exit sequence and timing requirements.

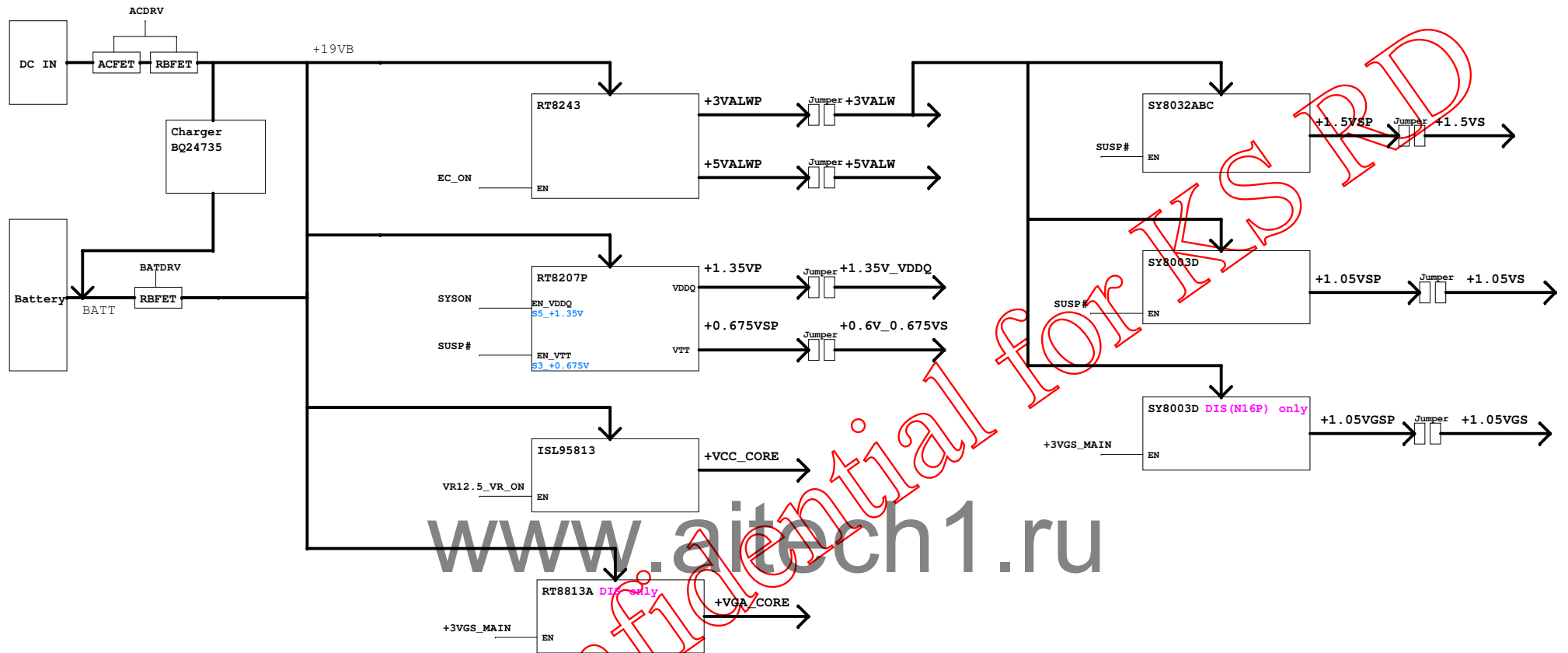
The diagram illustrates the timing sequence for GCS Entry and Exit. The signals shown are FB_CKE, PEX_LINK, GPU_PEX_RST#, GCS_FB_EN, 3V3_MAIN_EN, All Rail PGOOD, and GPU_EVENT#.

GCS Entry: FB_CKE transitions from Normal to Self-Refresh. PEX_LINK transitions from Active to X. GPU_PEX_RST# transitions from high to low. GCS_FB_EN transitions from high to low. 3V3_MAIN_EN transitions from high to low. All Rail PGOOD transitions from high to low. GPU_EVENT# transitions from high to low.

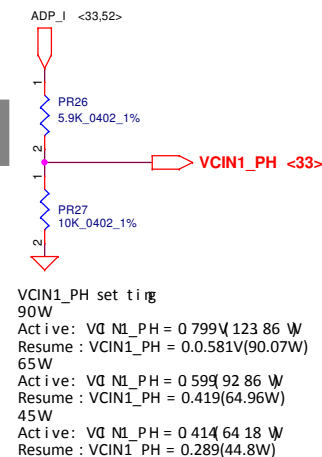
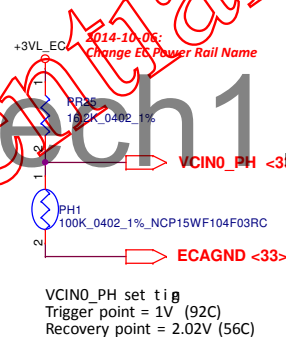
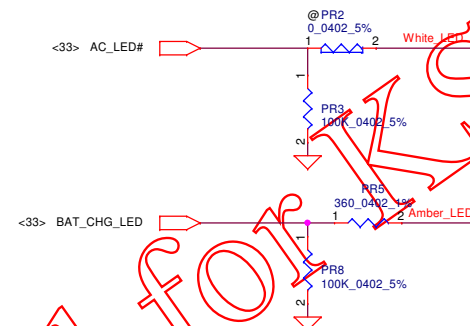
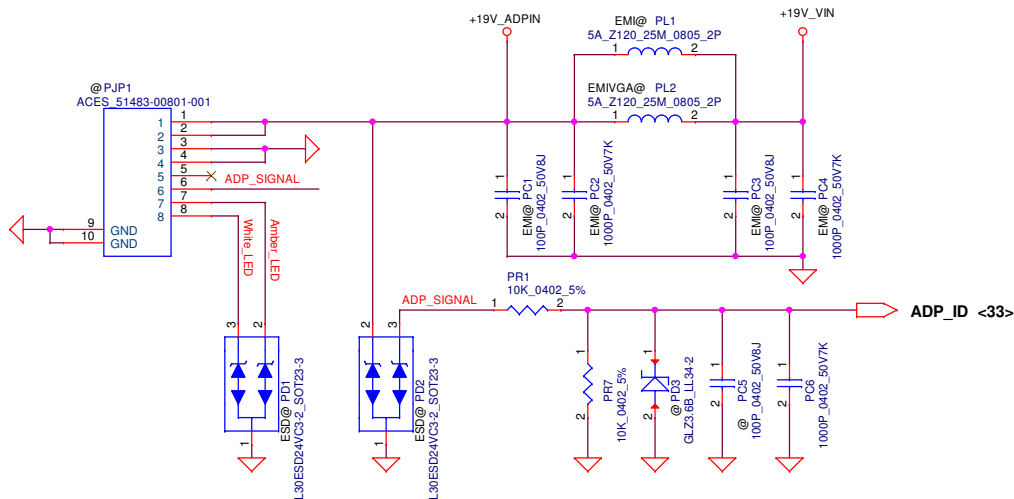
GCS Exit: FB_CKE transitions from Self-Refresh to Normal. PEX_LINK transitions from X to Detect and then to Train. GPU_PEX_RST# transitions from low to high. GCS_FB_EN transitions from low to high. 3V3_MAIN_EN transitions from low to high. All Rail PGOOD transitions from low to high. GPU_EVENT# transitions from low to high.

Timing parameters T1 and T0 are indicated. T1 is the time from 3V3_MAIN_EN rising to GPU_EVENT# rising. T0 is the time from GPU_EVENT# rising to GPU_PEX_RST# rising.

Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

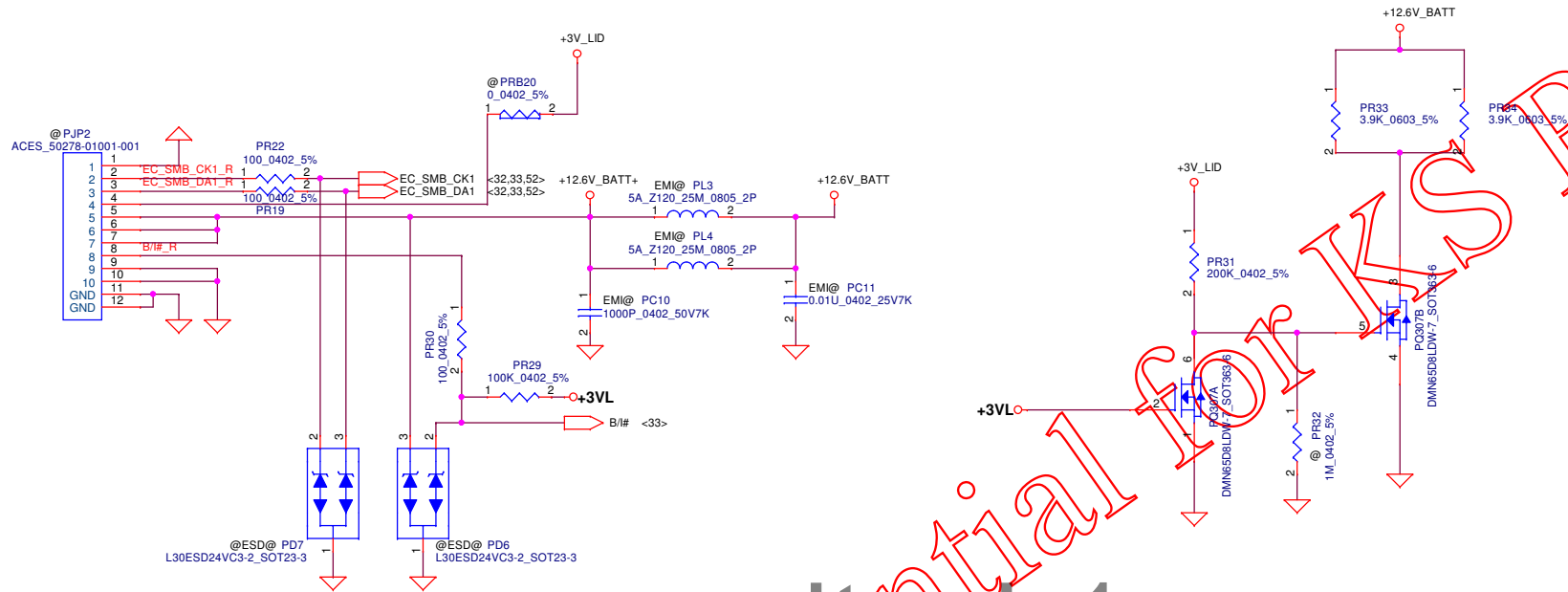


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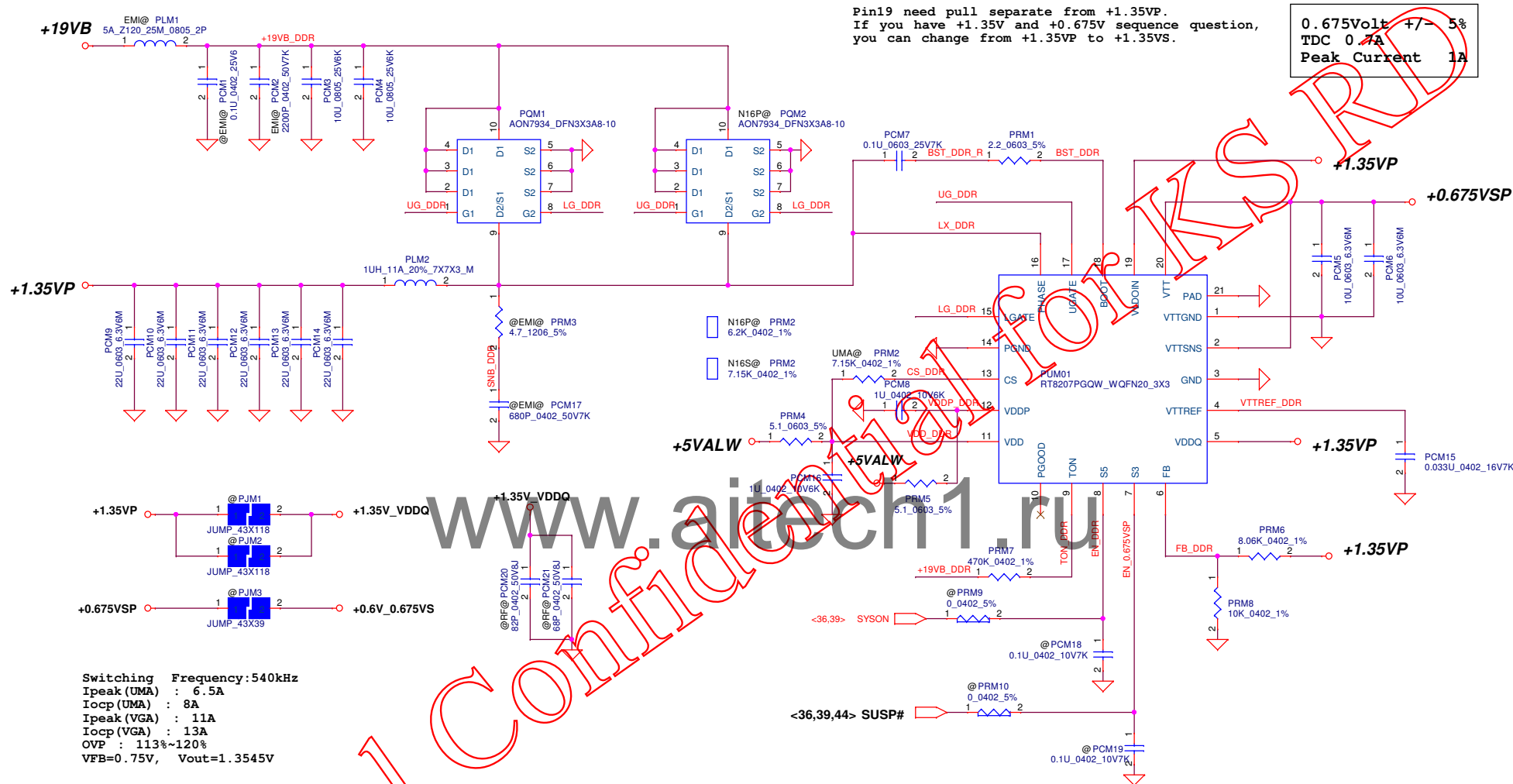
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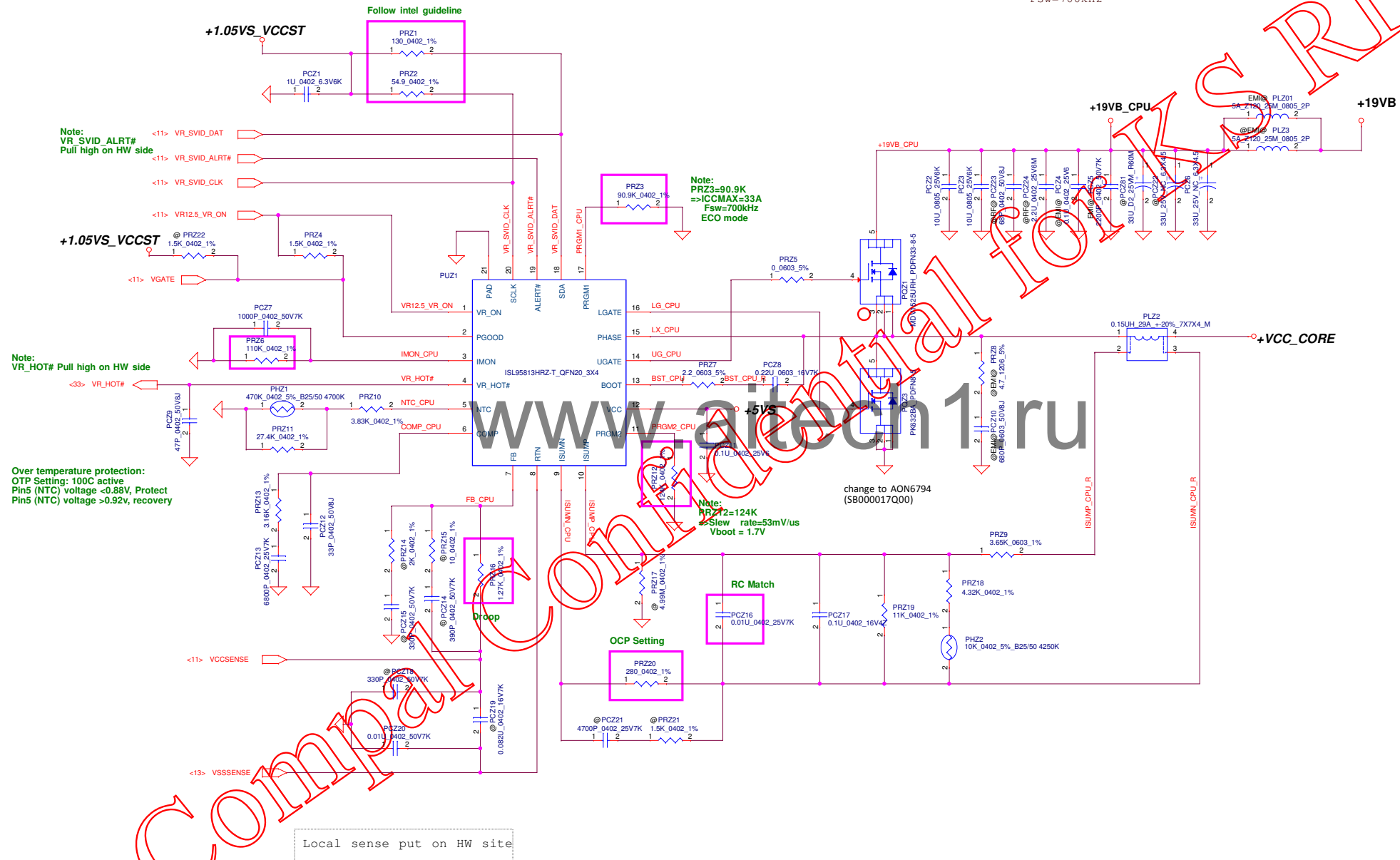
Module model information:
 ISL95813_V1A for IC module
 ISL95813_V1B for SW module

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

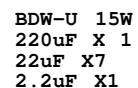
L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.15UH (Size:7*7*3)
Rdc=0.66mohm +-7%
Heat Rating Current=36A

ITDC=10A
ICCMAX=32A
OCP=38A
Fsw=700kHz

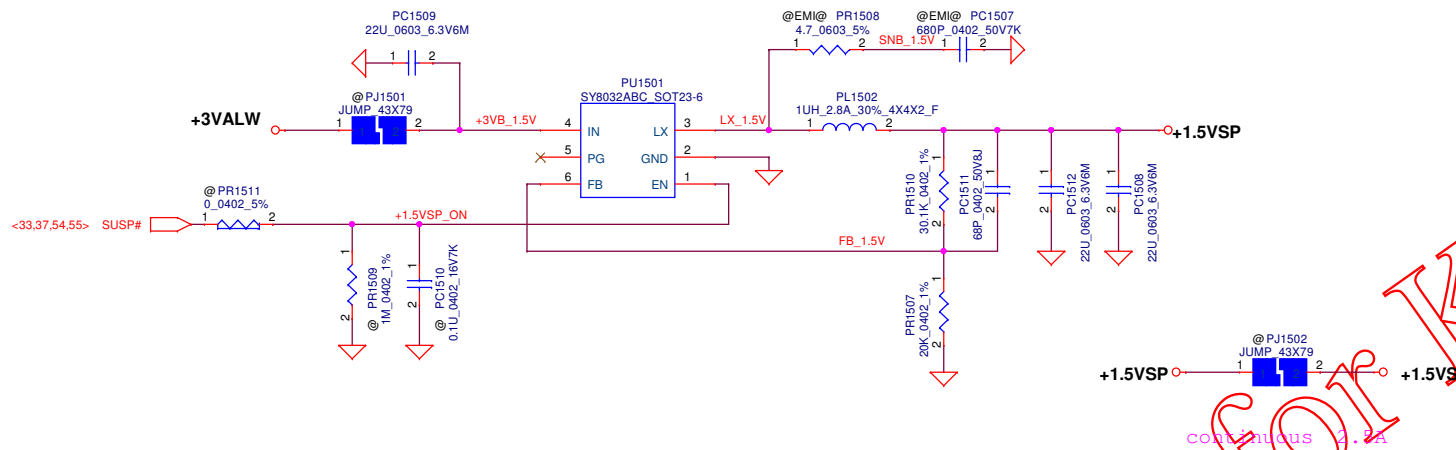


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H-side MOS: AON6992
Rds(on):
4.3mohm@Vgs=10V
5.2mohm@Vgs=4.5V
Id :32A@Tc=100C

L-side MOS: AOS6992
Rds(on):
2mohm@Vgs=10V
2.2mohm@Vgs=4.5V
Id :66A@Tc=100C

Choke: 0.22UH (Size:7*7*3)
Rdc=0.98mohm +5%
Heat Rating Current=28A

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

- VSNS Soft-Start time (Internal) is 0.7ms (PCV17 un-pop)
 $T_{ss} = (C_{ss} \cdot V_{refin}) / I_{ss} = 2.3ms$
 $= 0.01U \cdot 0.9V / 5uA = 2.3ms$ (PCV17 pop)
- Switching frequency setting:
 $F_{sw} = (V_{in} - 0.5) / (2 \cdot V_{in} \cdot R_{ton} \cdot 3.2p) = 353kHz$
- Thermal monitoring:
(VGPU_VREF-VTSNS)/PRV21=VTSNS/Rth

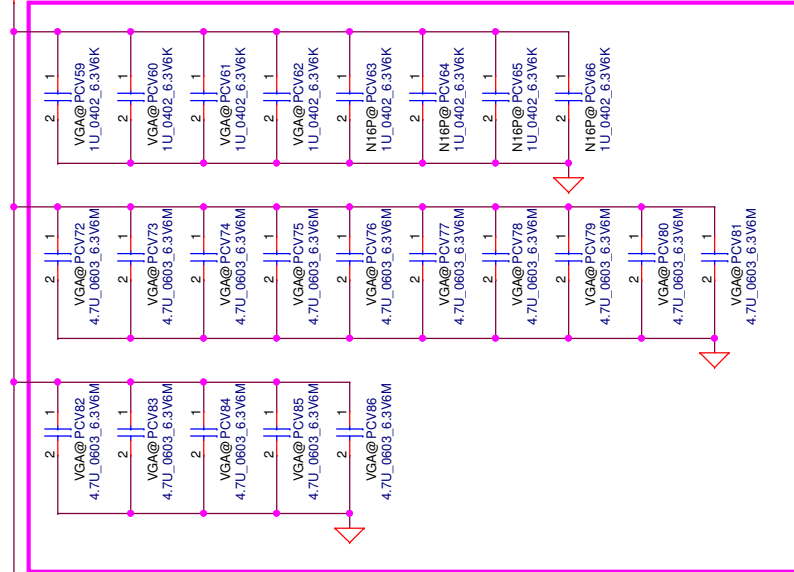
	T_min	T_typical	T_max
PRV21=18.7K	99.16C	101.57C	103.94C
PRV21=13K	110.19C	113.75C	115.26C
PRV21=8.2K	125.15C	127.91C	130.62C

Switching Frequency : 353kHz
I_{peak}(N16P-GT) : 70A
I_{ocp}(N16P-GT) : 83A
I_{peak}(N16S-GT) : 50A
I_{ocp}(N16S-GT) : 61A

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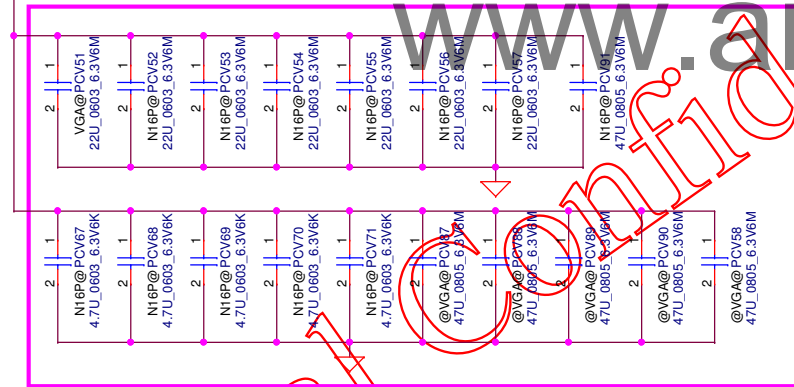
UNDER GPU



N16S-GT
330U 2V LESR6M H1.9 (SGA00001Q80) X 3
47U 6.3V X5R 0805 (SE000000PL00) X 1
22U 6.3V X5R 0603 (SE000000M000) X 1
4.7U 6.3V X5R 0603 H0.8 (SE107475M80) X 15
1U 6.3V X5R 0402 (SE000000K80) X 4

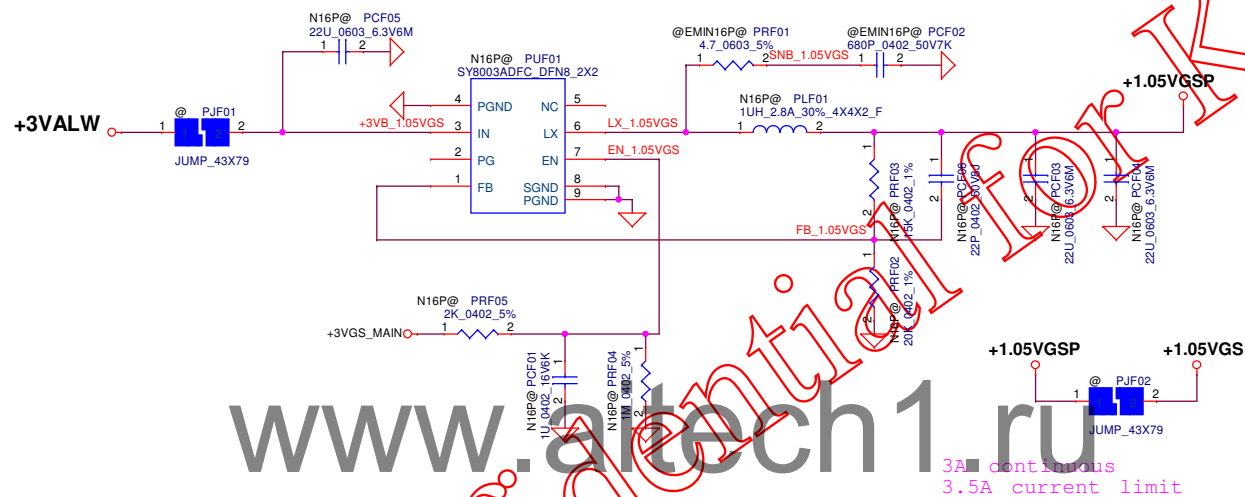
N16P-GT
330U 2V LESR6M H1.9 (SGA00001Q80) X 4
22U 6.3V X5R 0603 (SE000000M000) X 7
4.7U 6.3V X5R 0603 H0.8 (SE107475M80) X 15
4.7U 6.3V X5R 0603 (SE107475K80) X 5
1U 6.3V X5R 0402 (SE000000K80) X 8

NEAR GPU



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For Nvidia N16P-GT



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				Document Number	0.1
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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1							
2							
3							
4							

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Size	Document Number	Rev			
Custom	<Doc>	1.0			
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		ME request	0.2	P19	Change eDP Connector(JLCD1) for ME	12/15	
2		Screw Hole	0.2	P32	Change H20 from 3.0 mm to 3.3 mm	12/15	
3		Sub USB Power Switch	0.2	P26	Change Power Switch USB circuit	12/15	
4		ME Flash Circuit	0.2	P6	Add ME FLASH Circuit	12/15	
5		Audio GND Bridge circuit	0.2	P28	Add two Resistor for HP request	12/15	
6		Add JUMP on JUSB1 and JUSB2 Power	0.2	P26	Add JUMP JPV5	12/19	
7		ESD request	0.2	P34	Change Touch PAD Diode for ESD request	12/19	
8		ESD request	0.2	P19	Reserve Touch Screen Diode for ESD	12/19	
9		ESD request	0.2	P19	Change Camera and D-MIC Diode for ESD request	12/19	
10		Audio team Request	0.2	P28	Change JSPK2 Pin define	12/22	
11		Vendor Request	0.2	P31 P33	Change Subwoofer circuit	12/22	
12		Customer Request	0.2	P35 P33	Add Shipping Mode Circuit	12/22	
13		RF Request	0.2	P26 P32	Reserve 68P and 82P on +3VALW and +USB_VCC4	12/23	
14		ESD request	0.2	P20	Change HDMI EMI Solution	12/23	
15		HW Modify	0.2	P48	Change N16X 1.35V and 1.05V solution	12/25	
16		HW Modify	0.3	P48	Change N16X 1.35V and 1.05V solution	01/23	
17		HW Modify	1.0	P32	Add DH5 for storage Mode	04/02	
18		Vendor Request	1.0	P31	Change Subwoofer circuit	04/02	
19		HW Modify	1.0		Change 0 ohm to short pad. RC8,RC108,RC119,RC378, RT19,RT37,RA32,RA34, RA38,RA39,RA50,RA51, RT17 RT18,RTS4	04/13	

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				HW PIR	
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